Video Electronics Standards Association

VESA

Video Electronics Standards Association
920 Hillview Court, Suite 140
Milpitas, CA 95035

Phone: (408) 957-9270
Fax: (408) 957-9277

VTB-EXT Standard

VESA VIDEO TIMING BLOCK EXTENSION DATA STANDARD

Release A
November 24, 2003

Purpose

This standard defines data formats to carry configuration information, allowing optimum use of displays.

Summary

This document (Release A) describes version 1 of a 128-byte data structure known as the "Video Timing Block Extension (VTB-EXT)". The VTB-EXT data structure may contain up to six Detailed Timing Block (DTB) Descriptors, or up to 40 Coordinated Video Timing (CVT) Descriptors, or up to 61 Standard Timing (ST) Descriptors, or a combination of DTB, CVT and ST video timing descriptors. VTB-EXT requires the use of base EDID data structure version 1.3 (or newer). Use of VTB-EXT described in this document requires use of the addressing method described in the Enhanced DDC Standard (E-DDC).

Note

This issue of the VTB-EXT document contains specifications for the mandatory/optional data structures contained in this extension block. The base EDID data structure (version 1.3 or newer) is defined in a separate document.

SPECIAL NOTICE: There are several references to GTF in the VTB-EXT Standard. VESA is in the process of replacing the GTF Standard with the CVT Standard. When this occurs, all GTF references in the VTB-EXT Standard shall be replaced with CVT.

©Copyright 1994 - 2003 Video Electronics Standards Association

Preface

Intellectual Property

Copyright © 1994 - 2003 Video Electronics Standards Association. All rights reserved.

While every precaution has been taken in the preparation of this standard, the Video Electronics Standards Association and its contributors assume no responsibility for errors or omissions, and make no warranties, expressed or implied, of functionality or suitability for any purpose.

Trademarks

All trademarks used within this document are the property of their respective owners. VESA, DDC, EDID, GTF, CVT, etc. are trademarks of the Video Electronics Standard Association.

Patents

VESA proposals and standards are adopted by the Video Electronics Standards Association without regard as to whether their adoption may involve any patents or articles, materials, or processes. Such adoption does not assume any liability to any patent owner, nor does it assume any obligation whatsoever to parties adopting the proposals or standards documents.

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product, which incorporates EDID, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. All comments or reported errors should be submitted in writing to VESA using one of the following methods.

- Fax: 408-957 9277, *direct this note to Technical Support at VESA*
- e-mail: support@vesa.org
- mail: Technical Support
  Video Electronics Standards Association
  920 Hillview Court, Suite 140
  Milpitas, CA 95035
- website: www.vesa@org

Revision History

November 24, 2003 – Initial release of the standard.

Acknowledgments

This document would not have been possible without the efforts of the VESA Display Committee. In particular, the following individuals and their companies contributed significant time and knowledge to this edition of the VTB-EXT document.

Syed Athar Hussain	ATI Technologies Inc.
Don Chambers	Cables To Go
Takashi Matsui	EIZO NANAO
Graham Loveridge	Genesis Microchip
Jim Webb	Genesis Microchip
Susan Luerich	IBM
Ian Miller	Samsung
Steve Hasegawa	Sony

Workgroup Leader
Jack Hosek NEC-Mitsubishi

Document Editor
Alain d'Hautecourt ViewSonic

©Copyright 1994 - 2003 Video Electronics Standards Association

Table of Contents

REVISION HISTORY **3**

1. OVERVIEW **5**

1.1 SUMMARY 5
1.2 BACKGROUND 5
1.3 STANDARD OBJECTIVES 5
1.4 REFERENCE DOCUMENTS 6

2. VIDEO TIMING BLOCK EXTENSION (VTB-EXT) DATA STRUCTURE VER. 1 ... 7

2.1 VTB-EXT DATA STRUCTURE FORMAT OVERVIEW 8
2.2 TAG LABEL & VERSION NUMBER: 2 BYTES – ADDRESS/OFFSET 00H TO 01H 9
2.3 VTB-EXT DATA STRUCTURE LAYOUT: 3 BYTES – ADDRESS/OFFSET 02H TO 04H 9
2.4 DETAILED TIMING SECTION: 108 BYTES (MAXIMUM) 11
2.5 COORDINATED VIDEO TIMING (CVT) DESCRIPTORS – 120 BYTES (MAXIMUM) 14
2.6 STANDARD TIMING DESCRIPTORS – 122 BYTES (MAXIMUM) 16
2.7 UNUSED BYTES 17
2.8 CHECKSUM – 1 BYTE - ADDRESS/OFFSET 7FH 18

3. APPENDIX A – SAMPLE VTB-EXT BLOCK 19

3.1 EXAMPLE 1 - VTB-EXT BLOCK EX. - FOR REFERENCE ONLY (VER.1 DATA STRUCTURE) 19

4. APPENDIX B – NOTE REGARDING BORDERS – (FOR INFORMATION ONLY) **.. 28**

5. APPENDIX C – DATA FORMATS – (FOR INFORMATION ONLY) **..... 29**

5.1 VIDEO TIMING BLOCK EXTENSION (VTB-EXT) HIGH LEVEL LAYOUT 29
5.1.1 Mandatory elements 29
5.1.2 EDID Block Map Extension 30
5.1.3 General Extension Format 30

6. APPENDIX D – GLOSSARY 31

7. APPENDIX E - ANSWERS TO COMMONLY ASKED QUESTIONS 32

List of Tables

Table 2-1 – VTB-EXT Data Structure Version 1 8
Table 2-2 – Tag Label & Version Number 9
Table 2-3 – VTB-EXT Data Structure Layout 9
Table 2-4 - Detailed Timing Description 12
Table 2-5 - Decode of Stereo Mode Bits 13
Table 2-6 - Sync Signal Description 13
Table 2-7 – 3 Byte CVT Descriptor 15
Table 2-8 – 2 Byte Standard Timing Descriptors 17
Table 2-9 – Unused Bytes 17
Table 2-10 – Checksum 18
Table 5-1 – Extension Blocks – Mandatory Elements 29
Table 5-2 – EDID Block Map Extension 30
Table 5-3 – General Extension Format 30

©Copyright 1994 - 2003 Video Electronics Standards Association

1. OVERVIEW

1.1 Summary

The Enhanced EDID family of documents includes:

1. Enhanced EDID Standard (Basic 128-byte data structure. Rules for how EDID extensions are mapped.)
2. Enhanced EDID Implementation Guide
3. Optional EDID Extension Standards (data structures for additional data contained in EDID extensions are mapped).
    - 3.1 EDID Structure 2 Extension
    - 3.2 Display Information Extension (DI-EXT)
    - 3.3 CEA EDID Timing Extension (CE-EXT) – defined in EIA/CEA 861 Specifications
    - 3.4 …future extension structures not yet defined

1.2 Background

The use of a base (block 0) EDID in a display has become an integral requirement for "Plug & Play" in the display/graphics subsystem. The base EDID allows the host to identify the display as well as the display's capabilities. Video timing formats (Established Timings, Standard Timings, Preferred Timing Mode, GTF, etc.) are described in the base EDID. The base EDID has room for four detailed timing blocks. However, three of these blocks are typically used to satisfy other industry requirements. As a result, only one detailed timing block is available to describe a video timing format and this block is reserved for the preferred timing mode. In addition, the display industry has expanded the number and type of displays available in the marketplace. Many of these new displays require video timing formats which cannot be described in the current base EDID. Current base EDID data structure definitions are full and there is no room for expansion. The VTB-EXT Standard was developed to support these new displays by defining additional video timing formats. The VTB-EXT data structure may contain up to six Detailed Timing Block (DTB) Descriptors or up to 40 Coordinated Video Timing (CVT) Descriptors or up to 61 Standard Timing (ST) Descriptors or a combination of DTB, CVT & ST video timings. If the combination of DTB, CVT & ST video timings exceeds 122 bytes, then additional VTB-EXT data blocks can be used.

1.3 Standard Objectives

The VTB-EXT Standard was developed by VESA to meet, exceed and/or complement certain criteria. These criteria are set forth as Standard Objectives as follows:

- Support Microsoft® Plug and Play definition
- Provide information in a compact format to allow the graphics subsystem to be configured based on the capabilities of the attached display

©Copyright 1994 - 2003 Video Electronics Standards Association

1.4 Reference Documents

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

- VESA Coordinated Video Timings (CVT) Standard, Version 1, March 26, 2003
- VESA Enhanced Display Data Channel Standard (E-DDC), Version 1, September 2, 1999
- VESA Enhanced Extended Display Identification Standard (E-EDID), Release A, Revision 1., February 9, 2000
- VESA Enhanced Extended Display Identification Data Implementation Guide, Version 1.0, June 4, 2001
- VESA Generalized Timing Formula Standard (GTF), Version 1.0, December 18, 1996
- VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) – Version 1.0, Revision 0.8, September 17, 1998
- EIA/CEA-861-B, A DTV Profile for Uncompressed High Speed Digital Interfaces, date TBD.

©Copyright 1994 - 2003 Video Electronics Standards Association

2. Video Timing Block Extension (VTB-EXT) Data Structure Ver. 1

The Video Timing Block Extension (VTB-EXT) Data shall comply with the following rules:

1. The VTB-EXT is a 128-byte data structure which is an extension block to the base (block 0) EDID table. The VTB-EXT cannot stand alone and must be associated with a base EDID.
2. Use of the VTB-EXT described in this document requires that one of the addressing methods described in the Enhanced DDC Standard is used.
3. The VTB-EXT data structure may contain up to six Detailed Timing Block (DTB) Descriptors or up to 40 Coordinated Video Timing (CVT) Descriptors or up to 61 Standard Timing (ST) Descriptors or a combination of DTB, CVT & ST video timings. If the combination of DTB, CVT & ST video timings exceeds 122 bytes, then additional VTB-EXT data blocks can be used.
4. This standard advocates support of only detailed timings in the DTB 18-byte descriptors. Other types of data in 18-bytes descriptors, while allowed in the base EDID, shall not be allowed in the VTB-EXT.
5. Detailed timing blocks (DTB) follow the 18-byte format shown in the E-EDID standard. The DTB format is repeated in table 2-4 of this document. Refer to section 2.4.
6. Coordinated Video Timing (CVT) descriptions follow the 3-byte format shown in table 2-7 of this document. Refer to section 2.5.
7. Standard timings (ST) follow the 2-byte format shown the E-EDID standard. The ST format is repeated in table 2-8 of this document. Refer to section 2.6.
8. Timing priority by type of timing descriptor (DTB, CVT or ST) is defined in the E-EDID standard and should be used when user timing preference has not yet been established. Of the timings listed in this extension, detailed timings take priority over other types. Coordinated video timings take the next priority followed by standard timings. This follows the order in which they appear in this standard. Within each timing type, priority can be established by order as well. Higher priority timings should be placed first within each timing type.
9. All data must be sequentially stored starting with the first detailed timing block at address/offset '**05h**'. There cannot be any gaps between detailed timing blocks (DTB), coordinated video timing (CVT) descriptions or standard timing (ST) descriptions.
10. There may be unused bytes after all DTB, CVT and ST descriptors have been defined. Unused bytes in the VTB-EXT shall be filled with "00h".
11. All video timing data must represent video timing modes that are supported by the monitor.
12. Only one listing of a particular video timing format is allowed. Multiple listings of the same video timing format are not permitted.

Refer to table 2-1 for an outline of the VTB-EXT data structure.

©Copyright 1994 - 2003 Video Electronics Standards Association

2.1 VTB-EXT Data Structure Format Overview

Address/Offset	No. bytes	Description	Format
00h	**2**	**Tag Label & Version Number**	See Section 2.2
00h	1	'10h' = VTB-EXT Tag Label	
01h	1	'01h' = VTB-EXT Data Structure Version Number	
02h – 04h	**3**	**VTB-EXT Data Structure Layout**	See Section 2.3
02h	1	w = Number (in Hex) of Detailed Timing Blocks (DTB)	w ≤ 06h
03h	1	y = Number (in Hex) of Coordinated Video Timings (CVT) Descriptions	y ≤ 28h
04h	1	z = Number of Standard Timings (ST) Descriptions	z ≤ 3Dh
05h	**w*12h**	**Detailed Timing Block/s (DTB)**	See Section 2.4
05h	1	Data	18 bytes each description
06h	**…**	**…**	
…	…	**…**	
…	**…**	Data	
05h + w*12h	**y*03h**	**Coordinated Video Timing (CVT) Description/s**	See Section 2.5
05h + w*12h	1	Data	3 bytes each description
06h + w*12h	**…**	**…**	
07h + w*12h	…	**…**	
…	**…**	Data	
05h + w*12h + y*03h	**z*02h**	**Standard Timings (ST) Descriptions**	See Section 2.6
05h + w*12h + y*03h	1	Data	2 bytes each description
06h + w*12h + y*03h	1	**…**	
…	**…**	Data	
05h + w*12h + y*03h +z*02h	**7Ah – w*12h – y*03h – z*02h**	**Unused Byte - Reserved**	See Section 2.7
05h + w*12h + y*03h +z*02h	1	'00h' = All unused bytes shall be set to '00h'	
06h + w*12h + y*03h +z*02h	**…**	**…**	
…	**…**	**…**	
7Fh	**1**	**Checksum**	See Section 2.8
7Fh		'xxh' ⇒ The 1-byte sum (modulo 256) of all 128 bytes in this VTB-EXT block shall equal zero	

Table 2-1 – VTB-EXT Data Structure Version 1

Notes for Table 2-1: Refer to section 2.3 for more information on the w, y and z variables.
Examples of Address/Offset calculations:

1. A VTB-EXT Block with 4 DTBs, 3 CVTs and 6 STs defines w = 04h, y = 03h and z = 06h.

©Copyright 1994 - 2003 Video Electronics Standards Association

1.1 The starting address for the DTB section is **05h**.
1.2 The starting address for the CVT section is 05h + 04h∗12h = **4Dh.**
1.3 The starting address for the ST section is 05h + 04h∗12h + 03h∗03h = **56h.**
1.4 There will be 7Ah – 04h∗12h - 03h∗03h - 06h*02h = 1Dh = 29 (dec) Unused Bytes starting at address 05h + 04h∗12h + 03h∗03h + 06h*02h = **62h**.

2. A VTB-EXT Block with 5 DTBs, 0 CVTs and 9 STs defines w = 05h, y = 00h and z = 09h.
2.1 The starting address for the DTB section is **05h**.
2.2 There are no CVT descriptors.
2.3 The starting address for the ST section is 05h + 05h∗12h + 00h∗03h = **5Fh.**
2.4 There will be 7Ah – 05h∗12h - 00h∗03h - 09h*02h = 0Eh = 14 (dec) Unused Bytes starting at address 05h + 05h∗12h + 00h∗03h + 09h*02h = **71h**.

The following sections provide details on each byte of the VTB-EXT version 1 data structure.

2.2 Tag Label & Version Number: 2 bytes – Address/Offset 00h to 01h

The first two bytes of the VTB-EXT block include the Tag Label (‘10h’) and the data structure Version Number (‘01h’). The format is shown in Table 2.2.

Address/ Offset	2	Bytes	Data	Description
00h		1	‘10h’	Tag Label – defined by VESA
01h		1	‘01h’	Version Number 1

Table 2-2 – Tag Label & Version Number

2.3 VTB-EXT Data Structure Layout: 3 bytes – Address/offset 02h to 04h

The next 3 bytes define the number of 18 byte detailed timing blocks (DTB), the number of 3-byte coordinated video timing (CVT) descriptions and the number of 2 byte standard timing (ST) descriptions included in the VTB-EXT. The data format is shown in Table 2.3.

Address/ Offset	3	Bytes	Data	Description	Format
02h		1	‘w’	‘w’ = Number (in Hex) of Detailed Timing Blocks (DTB)	w must be less than or equal to 06h.
03h		1	‘y’	‘y’ = Number (in Hex) of Coordinated Video Timings (CVT) Descriptions	y must be less than or equal to 28h.
04h		1	‘z’	‘z’ = Number of Standard Timings (ST) Descriptions	z must be less than or equal to 3Dh.

Table 2-3 – VTB-EXT Data Structure Layout

The total space available for timing data within the VTB extension is 122 bytes.
The maximum number ‘w’ of 18-byte detailed timings (DTB) per VTB extension is 06h (6 dec).
The maximum number ‘y’ of 3-byte coordinated video timing (CVT) descriptors per VTB extension is 28h (40 dec).

©Copyright 1994 - 2003 Video Electronics Standards Association

The maximum number ‘z’ of 2-byte standard timings (ST) per VTB extension is 3Dh (61 dec). The total of w∗12h + y∗03h + z∗02h must be less than or equal to 7Ah (122 dec).

©Copyright 1994 - 2003 Video Electronics Standards Association

2.4 Detailed Timing Section: 108 bytes (maximum)

The detailed timing section can be divided to support up to 6 timing blocks, which are 18 bytes each. Up to six video timing formats can be stored in one VTB-EXT block. The detailed timing block section starts at address/offset '**05h**' and ends at '**04h + w*12h'** where '**w**' is the number (00h ≤ w ≤ 06h) of detailed timing blocks defined in the VTB-EXT. Refer to the VESA E-EDID Standard for the latest updates to the DTB descriptions.

The video timing format description for detailed timings is shown in Tables 2.4, 2.5 & 2.6. Use of the detailed timing block shall meet the following requirements.

1. The highest priority video timing format (listed in the VTB-EXT block) must be stored in the first detailed timing block (address **05h → 16h**). The lowest priority detailed timing video format must be stored in the last detailed timing block.
2. Any detailed timing outside of the monitor range limits (defined in base EDID) may cause the monitor to enter a self-protection mode (Out of Range). The host shall always verify that an intended video timing (listed in VTB-EXT) falls within the monitor range limits before the timing is applied to the monitor.
3. The preferred timing mode is the highest priority timing mode defined by the monitor manufacturer and must be listed in the first detailed timing block (address **36h → 47h**) in the base (block 0) EDID. The preferred timing mode must not be repeated in the VTB-EXT block.

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset						18 Bytes	Detailed Timing Descriptions	Format
DTB 1	DTB 2	DTB 3	DTB 4	DTB 5	DTB 6			
05h **06h**	**17h** **18h**	**29h** **2Ah**	**3Bh** **3Ch**	**4Dh** **4Eh**	**5Fh** **60h**	2	Pixel clock / 10,000	Stored LSB first. Example: 135MHz would be 13500 decimal, stored as BCh, 34h
07h	**19h**	**2Bh**	**3Dh**	**4Fh**	**61h**	1	Horizontal Active (HA)	Pixels, lower 8 bits of HA.
08h	**1Ah**	**2Ch**	**3Eh**	**50h**	**62h**	1	Horizontal Blanking (HBL)	Pixels, lower 8 bits of HBL.
09h	**1Bh**	**2Dh**	**3Fh**	**51h**	**63h**	1	Horizontal Active (HA): Horizontal Blanking (HBL)	Upper nibble : upper 4 bits of HA. Lower nibble : upper 4 bits of HBL.
0Ah	**1Ch**	**2Eh**	**40h**	**52h**	**64h**	1	Vertical Active (VA)	Lines, lower 8 bits of VA
0Bh	**1Dh**	**2Fh**	**41h**	**53h**	**65h**	1	Vertical Blanking (VBL)	Lines, lower 8 bits of VBL
0Ch	**1Eh**	**30h**	**42h**	**54h**	**66h**	1	Vertical Active (VA): Vertical Blanking (VBL)	Upper nibble : upper 4 bits of VA. Lower nibble : upper 4 bits of VBL.
0Dh	**1Fh**	**31h**	**43h**	**55h**	**67h**	1	Horizontal Sync. Offset (HSO)	Pixels , from blanking starts, lower 8 bits
0Eh	**20h**	**32h**	**44h**	**56h**	**68h**	1	Horizontal Sync Pulse Width (HSPW)	Pixels, lower 8 bits of HSPW
0Fh	**21h**	**33h**	**45h**	**57h**	**69h**	1	Vertical Sync Offset (VSO): Vertical Sync Pulse Width (VSPW)	Upper nibble : lines, lower 4 bits of VSO Lower nibble : lines, lower 4 bits of VSPW
10h	**22h**	**34h**	**46h**	**58h**	**6Ah**	1	Horizontal Sync Offset (HSO): Horizontal Sync Pulse Width (HSPW): Vertical Sync Offset (VSO): Vertical Sync Pulse Width (VSPW):	bits 7,6 : upper 2 bits of HSO bits 5,4 : upper 2 bits of HSPW bits 3,2 : upper 2 bits of VSO bits 1,0 : upper 2 bits of VSPW
11h	**23h**	**35h**	**47h**	**59h**	**6Bh**	1	Horizontal Image Size (HIS)	mm, lower 8 bits
12h	**24h**	**36h**	**48h**	**5Ah**	**6Ch**	1	Vertical Image Size (VIS)	mm, lower 8 bits
13h	**25h**	**37h**	**49h**	**5Bh**	**6Dh**	1	Horizontal Image Size (HIS): Vertical Image Size (VIS)	Upper nibble : upper 4 bits of HIS Lower nibble : upper 4 bits of VIS
14h	**26h**	**38h**	**4Ah**	**5Ch**	**6Eh**	1	Horizontal Border	Pixels, see Section 4
15h	**27h**	**39h**	**4Bh**	**5Dh**	**6Fh**	1	Vertical Border	Lines, see Section 4
16h	**28h**	**3Ah**	**4Ch**	**5Eh**	**70h**	1	Flags	Interlace, Stereo, Horizontal polarity, Vertical polarity, Sync Configuration, etc. Bit 7 Function 0 Non-interlaced 1 Interlaced Bit 6 Bit 5 Function 0 0 Normal display, no stereo x x See Table 2.5 for definition Bit 4 Bit 3 Function 0 0 Analog composite 0 1 Bipolar analog composite 1 0 Digital composite 1 1 Digital separate Bit 2 Bit 1 Function The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 2.6. Bit 0 See Table 2.5 for definition

Table 2-4 - Detailed Timing Description

©Copyright 1994 - 2003 Video Electronics Standards Association

Bit 6	Bit 5	Bit 0	Definition
0	0	x	Normal display, no stereo. The value of bit 0 is "don't care"
0	1	0	Field sequential stereo, right image when stereo sync. = 1
1	0	0	Field sequential stereo, left image when stereo sync. = 1
0	1	1	2-way interleaved stereo, right image on even lines
1	0	1	2-way interleaved stereo, left image on even lines
1	1	0	4-way interleaved stereo
1	1	1	Side-by-Side interleaved stereo

Table 2-5 - Decode of Stereo Mode Bits

The sync scheme for a detailed timing is described in bits 4-1 of the Flag byte. Bits 4 and 3 describe one of four schemes. Bits 2 and 1 give further details dependent on the values in bits 4 and 3. This is shown in Table 2.6.

Bits 4 and 3	Bit 2	Bit 2 Def.	Bit 1	Bit 1 Def.
0,0 Analog Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	On RGB	If set, sync pulses should appear on all 3 video signal lines. If not set, sync on green video line only.
0,1 Bipolar Analog Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	On RGB	If set, sync pulses should appear on all 3 video signal lines. If not set, sync on green video line only.
1,0 Digital Composite	Serrate	If set, controller shall supply serration (Hsync during Vsync).	Composite Polarity	This is the polarity of the Hsync pulses outside of Vsync. Polarity is positive if bit is set to 1
1,1 Digital Separate	Vertical Polarity	Vsync signal Polarity is Positive if bit is set to 1.	Horizontal Polarity	Hsync signal polarity is Positive if bit is set to 1.

Table 2-6 - Sync Signal Description

Notes for tables 2-4, 2-5 & 2-6:
Up to six detailed timing blocks/monitor descriptors (starting at address '**05h**') can be stored in one VTB-EXT. If less than six detailed timing blocks are required, the last detailed timing block is followed by the first coordinated video timing description (if required) or the first standard timing description (if required) or unused bytes section (if there are no CVT and no ST descriptors).

©Copyright 1994 - 2003 Video Electronics Standards Association

2.5 Coordinated Video Timing (CVT) Descriptors – 120 bytes (maximum)

The coordinated video timing (CVT) section can be divided to support up to 40 timing blocks, which are 3 bytes each. Up to 40 CVT formats can be stored in one VTB-EXT block. CVT descriptors must immediately follow the last detailed timing block (DTB) descriptor. The CVT section starts at address/offset '**05h + w∗12h'** and ends at '**04h + w∗12h + y∗03h'** where '**w**' is the number (00h ≤ w ≤ 06h) of detailed timing blocks and '**y**' is the number (00h ≤ y ≤ 28h) of coordinated video timing descriptors defined in the VTB-EXT. Table 2-7 provides a description of the 3 byte CVT codes. For more information on VESA CVT Standard, refer to the reference documents on page 6.

The video timing format description for CVT descriptors is shown in Tables 2.7. Use of the CVT descriptors shall meet the following requirements.

1. The highest priority CVT format (listed in the VTB-EXT block) must be stored in the first CVT descriptor block (address **05h + w∗12h → 07h + w∗12h**). The lowest priority CVT format must be stored in the last CVT block.
2. Any CVT format outside of the monitor range limits (defined in base EDID) may cause the monitor to enter a self-protection mode (Out of Range). The host shall always verify that an intended video timing (listed in VTB-EXT) falls within the monitor range limits before the timing is applied to the monitor.

Address/Offset	Byte #	Description	Comment
05h + w∗12h	1	**VSize LSbits**	Begin CVT Descriptor #1 Bits 7 – 0 defines the lower 8-bits of VSize. VSize is a 12-bit number that specifies (see equation) the number of active vertical lines in the supported timing format. Range of vertical active (VA) lines that can be defined is 2 to 8192. VSize = (Vertical Active/2) - 1 **Note**: CVT only supports an even number of active lines per frame.
06h + w∗12h	2	**VSize MSbits**	Upper nibble (bits 7 – 4) defines the upper 4-bits of VSize.
		Aspect Ratio	Bits 3 – 2 define the aspect ratio indicated by the following: Bits 3-2 Aspect Ratio 00 4:3 01 16:9 10 16:10 11 undefined (reserved) Together with VSize the aspect ratio will determine the pixel format.
		Reserved	Bits 1 - 0 are reserved and are set to '00'.
07h + w∗12h	3	**Reserved**	Bit 7 is reserved and is set to '0'.
		Preferred Refresh Rate	Bits 6 – 5 designates which of the supported refresh rates is preferred for the given format. This is indicated in the following: Bits 6 – 5 Preferred Rate 00 50Hz 01 60Hz 10 75Hz 11 85Hz An indication of 60Hz designates either 60Hz standard blanking or reduced blanking, whichever is supported. If both are supported the 60Hz indication means reduced blanking is preferred.

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset	Byte #	Description	Comment
			If the indicated preference does not correspond to a supported refresh rate than the highest refresh rate supported will be used as the preference.
		50Hz	Bit 4 set to 1 indicates that a 50Hz refresh rate with standard blanking (CRT style) is supported for the specified pixel format.
		60Hz	Bit 3 set to 1 indicates that a 60Hz refresh rate with standard blanking (CRT style) is supported for the specified pixel format.
		75Hz	Bit 2 set to 1 indicates that a 75Hz refresh rate with standard blanking (CRT style) is supported for the specified pixel format.
		85Hz	Bit 1 set to 1 indicates that an 85Hz refresh rate with standard blanking (CRT style) is supported for the specified pixel format.
		60Hz Reduced Blanking	Bit 0 set to 1 indicates that 60Hz Reduced Blanking timing (as per the CVT standard) is supported for the specified pixel format.
08h + w*12h	1	**VSize LSbits**	Begin CVT Descriptor #2
...	**...**	**...**	**...**
05h + w*12h + y*03h	1		Begin Standard Timings – See section 2.6

Table 2-7 – 3 Byte CVT Descriptor

Notes for table 2-7:

1.0 Active vertical size is used instead of horizontal size due to the following:

1.1 Using vertical size enables a compact way of expressing multiple aspect ratios. For example, a fixed format 16:9 display can center and display 4:3 and 16:10 timing which have the same number of active vertical lines without the need for scaling.

1.2 Due to cell width rounding of the horizontal resolution, it may not be possible to always accurately determine the correct number of active vertical lines. For example:

1360x768 is a recognized 16:9 format. If the vertical resolution is calculated using the horizontal resolution, a value of 765 is obtained, whereas using the vertical resolution and rounding to nearest cell width gives 1360.

The **active horizontal resolution** (**HActive**) is extracted by:

HActive = 8 ∗ {ROUNDDOWN [(**VActive** ∗ Aspect Ratio) / 8]}

Where: Aspect Ratio = 4:3, 16:9 or 16:10 (as specified in 3-byte CVT descriptor block)

ROUNDDOWN function rounds down to the nearest integer

Note: Timing that does not obey this rule is not CVT-compliant.

2.0 Each 3-byte CVT descriptor block allows the display to signal support for a single display format defined by the vertical size and aspect ratio. Within that block it is possible to indicate all CVT refresh rates supported at that format. The vertical refresh rates that can be supported include: 50Hz, 60Hz, 75Hz and 85Hz and 60Hz Reduced blanking.

3.0 Any coordinated video timing outside of the monitor range limits (defined in base EDID) may cause the monitor to enter a self-protection mode (Out of Range). The host shall always verify that an intended video timing (listed in VTB-EXT) falls within the monitor range limits before the timing is applied to the monitor.

©Copyright 1994 - 2003 Video Electronics Standards Association

2.6 Standard Timing Descriptors – 122 bytes (maximum)

The Standard Timing (ST) section can be divided to support up to 61 timing blocks, which are 2 bytes each. Up to 61 (if space is available) ST formats can be stored in one VTB-EXT block. ST descriptors must immediately follow the last coordinated video timing (CVT) descriptor. The ST section starts at address/offset '**05h + w∗12h + y∗03h**' and ends at '**04h + w∗12h + y∗03h + z∗02h**' where '**w**' is the number (00h ≤ **w** ≤ 06h) of detailed timing blocks, '**y**' is the number (00h ≤ **y** ≤ 28h) of coordinated video timing descriptors and '**z**' is the number (00h ≤ **z** ≤ 3Dh) of standard timings defined in the VTB-EXT block. Table 2-8 provides a description of the 2 byte ST codes. Refer to the VESA E-EDID Standard for the latest updates to the standard timing descriptions.

Each ST descriptor is identified by a unique 2-byte code derived from the mode format and refresh rate as described below. This scheme is used to identify future standard timings not included in the Established Timings section (refer to Section 3.8 of the E-EDID Standard). The use of standard timings in VTB-EXT shall meet the following requirements.
1. Standard Timings may be listed in VTB-EXT (starting at address/offset **05h + w∗12h + y∗03h**) only after all eight standard timings have been defined in the base (block 0) EDID. The eight standard timings with the highest priority must be listed (in order of priority) in the base EDID. Any remaining standard timings with lower priority may be stored (in order of priority) in the VTB-EXT block.
2. Standard Timing identifiers that correspond to a VESA Discrete Monitor Timing Mode are required to use the video timing formats defined in the "VESA and Industry Standards and Guidelines for Computer Display Monitor Timing" (version 1.0, revision 0.8 or newer). If a timing identifier listed corresponds to an issued VESA Discrete Monitor Timing, factory adjustment data must be stored (preset) in the display. Refer to reference document section on page 6.
3. Standard Timing identifiers that do not correspond to a VESA Discrete Monitor Timing Mode are required to use the "Generalized Timing Format" (GTF with default coefficients) to calculate the video timing format.
4. This scheme may also be used in monitors intended to be used exclusively with proprietary systems where the host already has the complete timing information.

Note: The 2-byte identifier codes for VESA standard timing modes are defined as part of each VESA Timing Standard.

The Standard Timings section is used to identify Factory Supported Modes that fall into one or both of two categories:
1. VESA Discrete Monitor Timings (listed in the VESA DMT Standard) not included in the current Established Timing section.
2. Discrete timing modes calculated (with default coefficients) using GTF.

The definition for standard timings is shown in table 2.8.

Factory Supported Modes **are defined as modes that are properly sized and centered as the monitor is delivered from the factory.**

All Factory Supported Modes are not necessarily listed in any EDID/VTB-EXT timing section.

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/ Offset	Byte #	Description	Comment
05h + w*12h + y*03h	1	**Horizontal Active Pixels (HAP) Indicator**	Begin Standard Timing Descriptor #9: Note: The first 8 standard timing descriptors must be listed in the base (block 0) EDID table. HAP Indicator = (Horizontal active pixels / 8) – 31 The range of horizontal active pixels that can be described in each byte is 256 → 2288 pixels, in increments of 8 pixels.
06h + w*12h + y*03h	2	**Image Aspect Ratio**	The vertical active line count may be calculated from the aspect ratio and the horizontal active pixel count given in the first byte. "Square" pixels (1:1 pixel aspect ratio) shall be assumed. Bit 7 Bit 6 Aspect Ratio 0 0 16:10 0 1 4:3 1 0 5:4 1 1 16:9 **Note:** EDID structures prior to Version 1 Revision 3 defined the bit combination of "00b" to indicate a 1:1 aspect ratio
		Refresh Rate (Hz)	Bits 5 → 0: Vertical refresh rate in Hz. Range is 60 → 123Hz
07h + w*12h + y*03h	1	**Horizontal Active Pixels (HAP) Indicator**	Begin Standard Timing Descriptor #10:
…	**…**	**…**	**…**
…	**…**	**…**	**…**
…	**…**	**…**	**…**
05h + w*12h + y*03h + z*02h	**…**	**Unused Bytes**	Begin Unused Byte Section: See section 2.7

Table 2-8 – 2 Byte Standard Timing Descriptors

2.7 Unused Bytes

The unused bytes are reserved and must be set to '00h'.

Address/Offset	Byte #	Description	Comments
05h + w*12h + y*03h + z*02h	**…**	**Unused Bytes** '00h'	Begin Unused Byte Section: '00h' = All unused bytes shall be set to '00h'
06h + w*12h + y*03h + z*02h	1	'00h'	**…**
07h + w*12h + y*03h + z*02h	1	'00h'	**…**
…	**…**	**…**	**…**
7Eh	**…**	**…**	**…**
7Fh	1	'xxh'	Checksum: See section 2.8

Table 2-9 – Unused Bytes

©Copyright 1994 - 2003 Video Electronics Standards Association

2.8 Checksum – 1 byte - Address/Offset 7Fh

This section indicates the checksum for the VTB-EXT block. Add all 128 bytes (in the VTB-EXT block) together using modulo 256 and the total is equal to ‘00h’.

Address/Offset	1	Byte	Data	Description
7Fh		1	‘xxh’	This byte should be programmed such that a one-byte checksum of the entire 128-byte DTB-EXT equals ‘00h’.

Table 2-10 – Checksum

©Copyright 1994 - 2003 Video Electronics Standards Association

3. APPENDIX A – Sample VTB-EXT Block

3.1 Example 1 - VTB-EXT block example - for reference only (Version 1 data structure)

This sample VTB-EXT block (version 1 data structure) is included for illustration only. It should not be considered as representative of any particular monitor. NOTE: All new monitors shall conform to base EDID data structure Version 1 Revision 3 (or newer). The video timing formats defined in this example are for a 3840x2400 (9.31 mega-pixel wide) LCD monitor. This example contains three DTB video timing formats, three CVT (Reduced Blanking) video timing formats, three CVT (Normal Blanking) video timing formats and three ST (using GTF) video timing formats. The CVT (Reduced Blanking) timings and the CVT (Normal Blanking) timings were calculated using the CVT Spreadsheet. The ST timings were calculated using the Generalized Timing Formula (GTF) Spreadsheet. The following are the 12 video timings listed in this example:
DTB1 ⇒ (Address/Offset **05h** to **16h**) 3840x2400 @ 13Hz vertical refresh (129.00MHz pixel clock) designated as 9.22MA.
DTB2 ⇒ (Address/Offset **17h** to **28h**) 3072x1920 @ 25.1Hz vertical refresh (157.00MHz pixel clock) designated as 5.90MA.
DTB3 ⇒ (Address/Offset **29h** to **3Ah**) 2456x1536 @ 39Hz vertical refresh (158.00MHz pixel clock) designated as 3.77MA.
CVT-RB1 ⇒ (Address/Offset **3Bh** to **3Dh**) 2304x1440 @ 60Hz (59.95Hz) vertical refresh (218.75MHz pixel clock) – Reduced Blanking - designated as 3.32MA-R.
CVT-RB2 ⇒ (Address/Offset **3Eh** to **40h**) 1920x1200 @ 60Hz (59.95Hz) vertical refresh (154.00MHz pixel clock) – Reduced Blanking - designated as 2.30MA-R.
CVT-RB3 ⇒ (Address/Offset **41h** to **43h**) 1728x1080 @ 60Hz (59.95Hz) vertical refresh (125.75MHz pixel clock) – Reduced Blanking - designated as 1.87MA-R.
CVT-NB4 ⇒ (Address/Offset **44h** to **46h**) 1152x720 @ 60Hz (59.972Hz) & 75Hz (74.721Hz) vertical refresh (66.75MHz & 85.75MHz pixel clocks, respectively) – Normal Blanking - designated as 0.83MA.
CVT-NB5 ⇒ (Address/Offset **47h** to **49h**) 960x600 @ 60Hz (59.635Hz) & 75Hz (74.842Hz) vertical refresh (42.25MHz & 58.75MHz pixel clocks, respectively) – Normal Blanking - designated as 0.58MA.
CVT-NB6 ⇒ (Address/Offset **4Ah** to **4Ch**) 768x480 @ 60Hz (59.896Hz) & 75Hz (74.710Hz) vertical refresh (28.75MHz & 36.75MHz pixel clocks, respectively) – Normal Blanking - designated as 0.37MA.
ST-9 ⇒ (Address/Offset **4Dh** to **4Eh**) 1680x1050 @ 60.00 Hz vertical refresh (147.136 MHz pixel clock) designated as 1.76MA.
ST-10 ⇒ (Address/Offset **4Fh** to **50h**) 1536x960 @ 60.00 Hz vertical refresh (122.143 MHz pixel clock) designated as 1.47MA.
ST-11 ⇒ (Address/Offset **51h** to **52h**) 1224x768 @ 60.00 Hz vertical refresh (76.702 MHz pixel clock) designated as 0.94MA.

All video timing formats are non-interlaced (progressive scan) and are non-stereo.

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value (hex)	Value (binary)	Field Name and *Comments*
Byte # (decimal)	Byte # (hex)			
0	**00**	10		⇒ VTB-EXT Block Tag Label is 10h
1	**01**	01		⇒ VTB-EXT Data Structure Version Number is 1
NOTE: The next 3 bytes define the number of DTB, CVT and ST descriptors.				
2	**02**	03		⇒ There are 3 detailed timing block (DTB) descriptors.
3	**03**	06		⇒ There are 6 coordinated video timing (CVT) descriptors.
4	**04**	03		⇒ There are 3 standard timing (ST) descriptors.
NOTE: **Start of DTB #1** ⇒ 3840x2400 @ 13 Hz vertical refresh (129.000 MHz pixel clock) – 9.22MA				
5	**05**	64		⇒ 3264 (hex) = 12900 (dec): Pixel Clock is 12900x10000 = 129.00 MHz.
6	**06**	32		Data is stored least significant byte first.
7	**07**	00	00000000	⇒ 1111~00000000 (bin) = 3840 (dec) Horizontal Active (HA) in pixels – lower 8 bits = 00 (hex). See address/offset **09h.**
8	**08**	00	00000000	⇒ 0001~00000000 (bin) = 256 (dec) Horizontal Blanking (HB) in pixels – lower 8 bits = 00 (hex). See address/offset **09h.**
9	**09**	F1	11110001	1111 (bin) ⇒ Upper nibble: upper 4 bits of HA. See address/offset **07h** and **08h.** 0001 (bin) ⇒ Lower nibble: upper 4 bits of HB. 11110001 (bin) = F1 (hex)
10	**0A**	60	01100000	⇒ 1001~01100000 (bin) = 2400 (dec) Vertical Active (VA) in lines – lower 8 bits = 60 (hex). See address/offset **0Ch.**
11	**0B**	16	00010110	⇒ 0000~00010110 (bin) = 22 (dec) Vertical Blanking (VB) in lines – lower 8 bits = 16 (hex). See address/offset **0Ch.**
12	**0C**	90	10010000	1001 (bin) ⇒ Upper nibble: upper 4 bits of VA. See address/offset **0Ah** and **0Bh.** 0000 (bin) ⇒ Lower nibble: upper 4 bits of VB. 10010000 (bin) = 90 (hex)
13	**0D**	20	00100000	⇒ 00~00100000 (bin) = 32 (dec) Horizontal Sync Offset (HSO) in pixels – from start of Horizontal Blanking (HB) to start of Horizontal Sync Pulse (HSP) – lower 8 bits = 20 (hex). See address/offset **10h.**
14	**0E**	80	10000000	⇒ 00~10000000 (bin) = 128 (dec) Horizontal Sync Pulse Width (HSPW) in pixels – lower 8 bits = 80 (hex). See address/offset **10h.**
15	**0F**	4A	01001010	⇒ 00~0100 (bin) = 4 (dec) Vertical Sync Offset (VSO) in lines – from start of Vertical Blanking (VB) to start of Vertical Sync Pulse (VSP) – upper nibble: lower 4 bits of VSO = 4 (hex), See address/offset **10h.** ⇒ 00~1010 (bin) = 10 (dec) Vertical Sync Pulse Width (VSPW) in lines-lower nibble: lower 4 bits of VSPW = A (hex). See address/offset **10h.**
16	**10**	00	00000000	⇒ Bits 7,6: 00 (bin) = upper 2 bits of HSO, ⇒ Bits 5,4: 00 (bin) = upper 2 bits of HSPW, ⇒ Bits 3,2: 00 (bin) = upper 2 bits of VSO, ⇒ Bits 1,0: 00 (bin) = upper 2 bits of VSPW See address/offset **0Dh, 0Eh** and **0Fh.**
17	**11**	DD	11011101	⇒ 0001~11011101 (bin) = 477 (dec) Horizontal Image Size (HIS) in mm – lower 8 bits = DD (hex). See address/offset **13h.**
18	**12**	29	00101001	⇒ 0001~00101001 (bin) = 297 (dec) Vertical Image Size (VIS) in mm – lower 8 bits = 29 (hex). See address/offset **13h.**

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value	Value	Field Name and *Comments*
Byte # (decimal)	**Byte # (hex)**	**Value (hex)**	**Value (binary)**	
19	**13**	11	00010001	⇒ 0001 (bin) = upper nibble: upper 4 bits of HIS, ⇒ 0001 (bin) = lower nibble: upper 4 bits of VIS, (See address/offset **11h** and **12h.**
20	**14**	00	00000000	⇒ 00000000 (bin) = 0 (dec) Horizontal Border in pixels
21	**15**	00	00000000	⇒ 00000000 (bin) = 0 (dec) Vertical Border in lines
22	**16**	1C	00011100	⇒ Bit 7: 0 (bin) indicates non-interlaced video ⇒ Bits 6 & 5: 00 (bin) indicates normal display, no stereo ⇒ Bits 4 & 3: 11 (bin) indicates digital separate syncs ⇒ Bits 2 & 1: 10 (bin) indicates vertical sync polarity is positive and horizontal sync polarity is negative. ⇒ Bit 0: 0 (bin) indicates normal display, no stereo
NOTE: **Start of DTB #2** ⇒ 3072x1920 @ 25.1 Hz vertical refresh (157.000 MHz pixel clock) – 5.90MA				
23	**17**	54		⇒ 3D54 (hex) = 15700 (dec): Pixel Clock is 15700x10000 = 157.00MHz.
24	**18**	3D		Data is stored least significant byte first.
25	**19**	00	00000000	⇒ 1100~00000000 (bin) = 3072 (dec) Horizontal Active (HA) in pixels – lower 8 bits = 00 (hex). See address/offset **1Bh.**
26	**1A**	78	01111000	⇒ 0000~01111000 (bin) = 120 (dec) Horizontal Blanking (HB) in pixels – lower 8 bits = 78 (hex). See address/offset **1Bh.**
27	**1B**	C0	11000000	1100 (bin) ⇒ Upper nibble: upper 4 bits of HA. See address/offset **19h** and **1Ah.** 0000 (bin) ⇒ Lower nibble: upper 4 bits of HB. 11110001 (bin) = C0 (hex)
28	**1C**	80	10000000	⇒ 0111~10000000 (bin) = 1920 (dec) Vertical Active (VA) in lines – lower 8 bits = 80 (hex). See address/offset **1Eh.**
29	**1D**	28	00101000	⇒ 0000~00101000 (bin) = 40 (dec) Vertical Blanking (VB) in lines – lower 8 bits = 28 (hex). See address/offset **1Eh.**
30	**1E**	70	01110000	0111 (bin) ⇒ Upper nibble: upper 4 bits of VA. See address/offset **1Ch** & **1Dh.** 0000 (bin) ⇒ Lower nibble: upper 4 bits of VB. 01110000 (bin) = 70 (hex)
31	**1F**	10	00010000	⇒ 00~00010000 (bin) = 16 (dec) Horizontal Sync Offset (HSO) in pixels – from start of Horizontal Blanking (HB) to start of Horizontal Sync Pulse (HSP) – lower 8 bits = 10 (hex). See address/offset **22h.**
32	**20**	40	01000000	⇒ 00~01000000 (bin) = 64 (dec) Horizontal Sync Pulse Width (HSPW) in pixels – lower 8 bits = 40 (hex). See address/offset **22h.**
33	**21**	AC	10101100	⇒ 00~1010 (bin) = 10 (dec) Vertical Sync Offset (VSO) in lines – from start of Vertical Blanking (VB) to start of Vertical Sync Pulse (VSP) – upper nibble: lower 4 bits of VSO = A (hex), See address/offset **22h.** ⇒ 00~1100 (bin) = 12 (dec) Vertical Sync Pulse Width (VSPW) in lines - lower nibble: lower 4 bits of VSPW = C (hex). See address/offset **22h.**
34	**22**	00	00000000	Bits 7,6: 00 (bin) = upper 2 bits of HSO, Bits 5,4: 00 (bin) = upper 2 bits of HSPW, Bits 3,2: 00 (bin) = upper 2 bits of VSO, Bits 1,0: 00 (bin) = upper 2 bits of VSPW See address/offset **1Fh, 20h** and **21h.**

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value	Value	Field Name and *Comments*
Byte # (decimal)	Byte # (hex)	(hex)	(binary)	
35	**23**	DD	11011101	⇒ 0001~11011101 (bin) = 477 (dec) Horizontal Image Size (HIS) in mm – lower 8 bits = DD (hex). See address/offset **25h.**
36	**24**	29	00101001	⇒ 0001~00101001 (bin) = 297 (dec) Vertical Image Size (VIS) in mm – lower 8 bits = 29 (hex). See address/offset **25h.**
37	**25**	11	00010001	⇒ 0001 (bin) = upper nibble: upper 4 bits of HIS, ⇒ 0001 (bin) = lower nibble: upper 4 bits of VIS, (See address/offset **23h** and **24h.**
38	**26**	00	00000000	⇒ 00000000 (bin) = 0 (dec) Horizontal Border in pixels
39	**27**	00	00000000	⇒ 00000000 (bin) = 0 (dec) Vertical Border in lines
40	**28**	1C	00011100	⇒ Bit 7: 0 (bin) indicates non-interlaced video ⇒ Bits 6 & 5: 00 (bin) indicates normal display, no stereo ⇒ Bits 4 & 3: 11 (bin) indicates digital separate syncs ⇒ Bits 2 & 1: 10 (bin) indicates horizontal sync polarity is negative and vertical sync polarity is positive ⇒ Bit 0: 0 (bin) indicates normal display, no stereo
NOTE: **Start of DTB #3** ⇒ 2456x1536 @ 39 Hz vertical refresh (158.000 MHz pixel clock) – designated as 3.77MA				
41	**29**	B8		⇒ 3DB8 (hex) = 15800 (dec): Pixel Clock is 15800x10000 = 158.00 MHz.
42	**2A**	3D		Data is stored least significant byte first.
43	**2B**	98	10011000	⇒ 1001~10011000 (bin) = 2456 (dec) Horizontal Active (HA) in pixels – lower 8 bits = 98 (hex). See address/offset **2Dh.**
44	**2C**	78	01111000	⇒ 0000~01111000 (bin) = 120 (dec) Horizontal Blanking (HB) in pixels – lower 8 bits = 78 (hex). See address/offset **2Dh.**
45	**2D**	90	10010000	1001 (bin) ⇒ Upper nibble: upper 4 bits of HA. 0000 (bin) ⇒ Lower nibble: upper 4 bits of HB. 10010000 (bin) = 90 (hex) See address/offset **2Bh** and **2Ch.**
46	**2E**	00	00000000	⇒ 0110~00000000 (bin) = 1536 (dec) Vertical Active (VA) in lines – lower 8 bits = 00 (hex). See address/offset **30h.**
47	**2F**	24	00100100	⇒ 0000~00100100 (bin) = 36 (dec) Vertical Blanking (VB) in lines – lower 8 bits = 24 (hex). See address/offset **30h.**
48	**30**	60	01100000	0110 (bin) ⇒ Upper nibble: upper 4 bits of VA. 0000 (bin) ⇒ Lower nibble: upper 4 bits of VB. 01100000 (bin) = 60 (hex) See address/offset **2Eh** and **2Fh.**
49	**31**	10	00010000	⇒ 00~00010000 (bin) = 16 (dec) Horizontal Sync Offset (HSO) in pixels - from start of Horizontal Blanking (HB) to start of Horizontal Sync Pulse (HSP) – lower 8 bits = 10 (hex). See address/offset **34h.**
50	**32**	40	01000000	⇒ 00~01000000 (bin) = 64 (dec) Horizontal Sync Pulse Width (HSPW) in pixels – lower 8 bits = 40 (hex). See address/offset **34h.**
51	**33**	A8	10101000	⇒ 00~1010 (bin) = 10 (dec) Vertical Sync Offset (VSO) in lines – from start of Vertical Blanking (VB) to start of Vertical Sync Pulse (VSP) in lines – upper nibble: lower 4 bits of VSO, See address/offset **34h.** ⇒ 00~1000 (bin) = 8 (dec) Vertical Sync Pulse Width (VSPW) in lines – lower nibble: lower 4 bits of VSPW = A8. See address/offset **34h.**

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value	Value	Field Name and *Comments*
Byte # (decimal)	**Byte # (hex)**	**Value (hex)**	**Value (binary)**	
52	**34**	00	00000000	⇒ Bits 7,6: 00 (bin) = upper 2 bits of HSO, ⇒ Bits 5,4: 00 (bin) = upper 2 bits of HSPW, ⇒ Bits 3,2: 00 (bin) = upper 2 bits of VSO, ⇒ Bits 1,0: 00 (bin) = upper 2 bits of VSPW See address/offset **31h, 32h** and **33h.**
53	**35**	DD	11011101	⇒ 0001~11011101 (bin) = 477 (dec) Horizontal Image Size (HIS) in mm – lower 8 bits = DD (hex). See address/offset **37h.**
54	**36**	29	00101001	⇒ 0001~00101001 (bin) = 297 (dec) Vertical Image Size (VIS) in mm – lower 8 bits = 29 (hex). See address/offset **37h.**
55	**37**	11	00010001	⇒ 0001 (bin) = upper nibble: upper 4 bits of HIS, ⇒ 0001 (bin) = lower nibble: upper 4 bits of VIS = 11 (hex) See address/offset **35h** and **36h.**
56	**38**	00	00000000	⇒ 00000000 (bin) = 0 (dec) Horizontal Border in pixels
57	**39**	00	00000000	⇒ 00000000 (bin) = 0 (dec) Vertical Border in lines
58	**3A**	1C	00011100	⇒ Bit 7: 0 (bin) indicates Non-interlaced video ⇒ Bits 6 & 5: 00 (bin) indicates Normal display, no stereo ⇒ Bits 4 & 3: 11 (bin) indicates Digital separate syncs ⇒ Bits 2 & 1: 10 (bin) indicates Horizontal sync polarity is negative and vertical sync polarity is positive ⇒ Bit 0: 0 (bin) indicates Normal display, no stereo
NOTE: **Start of CVT-RB #1** ⇒ 2304x1440 @ 59.945 Hz vertical refresh (218.750 MHz pixel clock) – Reduced Blanking – Designated as 3.32 MA-R.				
59	**3B**	CF	11001111	⇒ 0010~11001111 (bin) = 02~CF (hex) = 719 (dec) = VSize: Vertical Active (VA) = 1440 (dec): VSize = (VA/2) – 1 = (1440/2) – 1 = 719 (dec) = 02CF (hex). See address/offset **3Ch.**
60	**3C**	28	00101000	⇒ Bits 7 → 4: 0010 (bin) = upper nibble = upper 4 bits of VSize. See address/offset **3Bh.** ⇒ Bits 3 & 2: 10 (bin) = aspect ratio is 16:10 ⇒ Bits 1 & 0: 00 (bin) = reserved: 00101000 (bin) = 28 (hex)
61	**3D**	21	00100001	⇒ Bit 7: 0 (bin) = reserved ⇒ Bits 6 & 5: 01 (bin) indicates 60 Hz is the preferred vertical refresh rate, ⇒ Bit 4: 0 (bin) indicates 50 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 3: 0 (bin) indicates 60 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 2: 0 (bin) indicates 75 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 1: 0 (bin) indicates 85 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 0: 1 (bin) indicates 60 Hz vertical refresh rate (reduced blanking) is supported: 00100001 (bin) = 21 (hex).
NOTE: **Start of CVT-RB #2** ⇒ 1920x1200 @ 59.950 Hz vertical refresh (154.000 MHz pixel clock) – Reduced Blanking – Designated as 2.30MA-R.				

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value	Value	Field Name and *Comments*
Byte # (decimal)	**Byte # (hex)**	**Value (hex)**	**Value (binary)**	
62	**3E**	57	01011111	⇒ 0010~01011111 (bin) = 02~57 (hex) = 599 (dec) = VSize: Vertical Active (VA) = 1200 (dec): VSize = (VA/2) – 1 = (1200/2) – 1 = 599 (dec) = 0257 (hex). See address/offset **3Fh.**
63	**3F**	28	00101000	⇒ Bits 7 → 4: 0010 (bin) = upper nibble = upper 4 bits of VSize. See address/offset **3Eh.** ⇒ Bits 3 & 2: 10 (bin) = aspect ratio is 16:10 ⇒ Bits 1 & 0: 00 (bin) = reserved: 00101000 (bin) = 28 (hex)
64	**40**	21	00100001	⇒ Bit 7: 0 (bin) = reserved ⇒ Bits 6 & 5: 01 (bin) indicates 60 Hz is the preferred vertical refresh rate, ⇒ Bit 4: 0 (bin) indicates 50 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 3: 0 (bin) indicates 60 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 2: 0 (bin) indicates 75 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 1: 0 (bin) indicates 85 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 0: 1 (bin) indicates 60 Hz vertical refresh rate (reduced blanking) is supported: 00100001 (bin) = 21 (hex).
NOTE: **Start of CVT-RB #3** ⇒ 1728x1080 @ 59.950 Hz vertical refresh (125.750 MHz pixel clock) – Reduced Blanking – Designated as 1.87MA-R.				
65	**41**	1B	00011011	⇒ 0010~00011011 (bin) = 02~1B (hex) = 539 (dec) = VSize: Vertical Active (VA) = 1080 (dec): VSize = (VA/2) – 1 = (1080/2) – 1 = 539 (dec) = 021B (hex). See address/offset **42h.**
66	**42**	28	00101000	⇒ Bits 7 → 4: 0010 (bin) = upper nibble = upper 4 bits of VSize. See address/offset **41h.** ⇒ Bits 3 & 2: 10 (bin) = aspect ratio is 16:10 ⇒ Bits 1 & 0: 00 (bin) = reserved: 00101000 (bin) = 28 (hex)
67	**43**	21	00100001	⇒ Bit 7: 0 (bin) = reserved ⇒ Bits 6 & 5: 01 (bin) indicates 60 Hz is the preferred vertical refresh rate, ⇒ Bit 4: 0 (bin) indicates 50 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 3: 0 (bin) indicates 60 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 2: 0 (bin) indicates 75 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 1: 0 (bin) indicates 85 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 0: 1 (bin) indicates 60 Hz vertical refresh rate (reduced blanking) is supported: 00100001 (bin) = 21 (hex).
NOTE: **Start of CVT-NB #4** ⇒ 1152x720 @ 59.972 Hz & 74.721 Hz vertical refresh (66.750 MHz & 85.750 MHz pixel clock, respectively) – Normal Blanking – Designated as 0.83MA.				

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value	Value	Field Name and *Comments*
Byte # (decimal)	**Byte # (hex)**	**Value (hex)**	**Value (binary)**	
68	**44**	67	01100111	⇒ 0001~01100111 (bin) = 01~67 (hex) = 359 (dec) = VSize: Vertical Active (VA) = 720 (dec): VSize = (VA/2) – 1 = (720/2) – 1 = 359 (dec) = 0167 (hex). See address/offset **45h.**
69	**45**	18	00011000	⇒ Bits 7 → 4: 0001 (bin) = upper nibble = upper 4 bits of VSize. See address/offset **44h.** ⇒ Bits 3 & 2: 10 (bin) = aspect ratio is 16:10 ⇒ Bits 1 & 0: 00 (bin) = reserved: 00011000 (bin) = 18 (hex)
70	**46**	2C	00101100	⇒ Bit 7: 0 (bin) = reserved ⇒ Bits 6 & 5: 01 (bin) indicates 60 Hz is the preferred vertical refresh rate, ⇒ Bit 4: 0 (bin) indicates 50 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 3: 1 (bin) indicates 60 Hz vertical refresh rate (standard blanking) is supported, ⇒ Bit 2: 1 (bin) indicates 75 Hz vertical refresh rate (standard blanking) is supported, ⇒ Bit 1: 0 (bin) indicates 85 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 0: 0 (bin) indicates 60 Hz vertical refresh rate (reduced blanking) is not supported: 00101100 (bin) = 2C (hex).
NOTE: **Start of CVT-NB #5** ⇒ 960x600 @ 59.635 Hz & 74.842 Hz vertical refresh (45.250 MHz & 58.750 MHz pixel clock, respectively) – Normal Blanking – Designated as 0.58MA.				
71	**47**	2B	00101011	⇒ 0001~00101011 (bin) = 01~2B (hex) = 299 (dec) = VSize: Vertical Active (VA) = 600 (dec): VSize = (VA/2) – 1 = (600/2) – 1 = 299 (dec) = 012B (hex). See address/offset **48h.**
72	**48**	18	00011000	⇒ Bits 7 → 4: 0001 (bin) = upper nibble = upper 4 bits of VSize. See address/offset **47h.** ⇒ Bits 3 & 2: 10 (bin) = aspect ratio is 16:10 ⇒ Bits 1 & 0: 00 (bin) = reserved: 00011000 (bin) = 18 (hex)
73	**49**	2C	00101100	⇒ Bit 7: 0 (bin) = reserved ⇒ Bits 6 & 5: 01 (bin) indicates 60 Hz is the preferred vertical refresh rate, ⇒ Bit 4: 0 (bin) indicates 50 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 3: 1 (bin) indicates 60 Hz vertical refresh rate (standard blanking) is supported, ⇒ Bit 2: 1 (bin) indicates 75 Hz vertical refresh rate (standard blanking) is supported, ⇒ Bit 1: 0 (bin) indicates 85 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 0: 0 (bin) indicates 60 Hz vertical refresh rate (reduced blanking) is not supported: 00101100 (bin) = 2C (hex).
NOTE: **Start of CVT-NB #6** ⇒ 768x480 @ 59.896 Hz & 74.710 Hz vertical refresh (28.750 MHz & 36.750 MHz pixel clock, respectively) – Normal Blanking – Designated as 0.37MA.				

©Copyright 1994 - 2003 Video Electronics Standards Association

Address/Offset		Value	Value	Field Name and *Comments*
Byte # (decimal)	**Byte # (hex)**	**Value (hex)**	**Value (binary)**	
74	**4A**	EF	11101111	⇒ 0000~11101111 (bin) = 00~EF (hex) = 239 (dec) = VSize: Vertical Active (VA) = 480 (dec): VSize = (VA/2) – 1 = (480/2) – 1 = 239 (dec) = 00EF (hex). See address/offset **48h.**
75	**4B**	08	00001000	⇒ Bits 7 → 4: 0000 (bin) = upper nibble = upper 4 bits of VSize. See address/offset **47h.** ⇒ Bits 3 & 2: 10 (bin) = aspect ratio is 16:10 ⇒ Bits 1 & 0: 00 (bin) = reserved: 00011000 (bin) = 18 (hex)
76	**4C**	2C	00101100	⇒ Bit 7: 0 (bin) = reserved ⇒ Bits 6 & 5: 01 (bin) indicates 60 Hz is the preferred vertical refresh rate, ⇒ Bit 4: 0 (bin) indicates 50 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 3: 1 (bin) indicates 60 Hz vertical refresh rate (standard blanking) is supported, ⇒ Bit 2: 1 (bin) indicates 75 Hz vertical refresh rate (standard blanking) is supported, ⇒ Bit 1: 0 (bin) indicates 85 Hz vertical refresh rate (standard blanking) is not supported, ⇒ Bit 0: 0 (bin) indicates 60 Hz vertical refresh rate (reduced blanking) is not supported: 00101100 (bin) = 2C (hex).
NOTE: Start of ST #9 ⇒ 1680x1050 @ 59.950 Hz vertical refresh (125.750 MHz pixel clock) – Designated as 1.87MA. Note: ST video timing parameters calculated using GTF.				
77	**4D**	B3		⇒ Horizontal Active Pixels (HAP) Indicator = 1680 (HA)/8 – 31 = 179 (dec) = B3 (hex)
78	**4E**	3C	00111100	⇒ Bits 7 & 6: 00 (bin) indicates 16:10 aspect ratio ⇒ Bits 5 → 0: 111100 (bin) indicates 60 Hz vertical refresh rate: 00111100 (bin) = 3C (hex)
NOTE: Start of ST #10 ⇒ 1536x960 @ 60.00 Hz vertical refresh (122.143 MHz pixel clock) – Designated as 1.47MA. Note: ST video timing parameters calculated using GTF.				
79	**4F**	A1		⇒ Horizontal Active Pixels (HAP) Indicator = 1536 (HA)/8 – 31 = 161 (dec) = A1 (hex)
80	**50**	3C	00111100	⇒ Bits 7 & 6: 00 (bin) indicates 16:10 aspect ratio ⇒ Bits 5 → 0: 111100 (bin) indicates 60 Hz vertical refresh rate: 00111100 (bin) = 3C (hex)
NOTE: Start of ST #11 ⇒ 1224x768 @ 60.00 Hz vertical refresh (76.702 MHz pixel clock) – Designated as 0.94MA. Note: ST video timing parameters calculated using GTF.				
81	**51**	7A		⇒ Horizontal Active Pixels (HAP) Indicator = 1224 (HA)/8 – 31 = 161 (dec) = 7A (hex)
82	**52**	3C	00111100	⇒ Bits 7 & 6: 00 (bin) indicates 16:10 aspect ratio ⇒ Bits 5 → 0: 111100 (bin) indicates 60 Hz vertical refresh rate: 00111100 (bin) = 3C (hex)
83 … …	**53** … …	00 … …		⇒ 00 (bin): 45 (dec) unused bytes … …

©Copyright 1994 - 2003 Video Electronics Standards Association

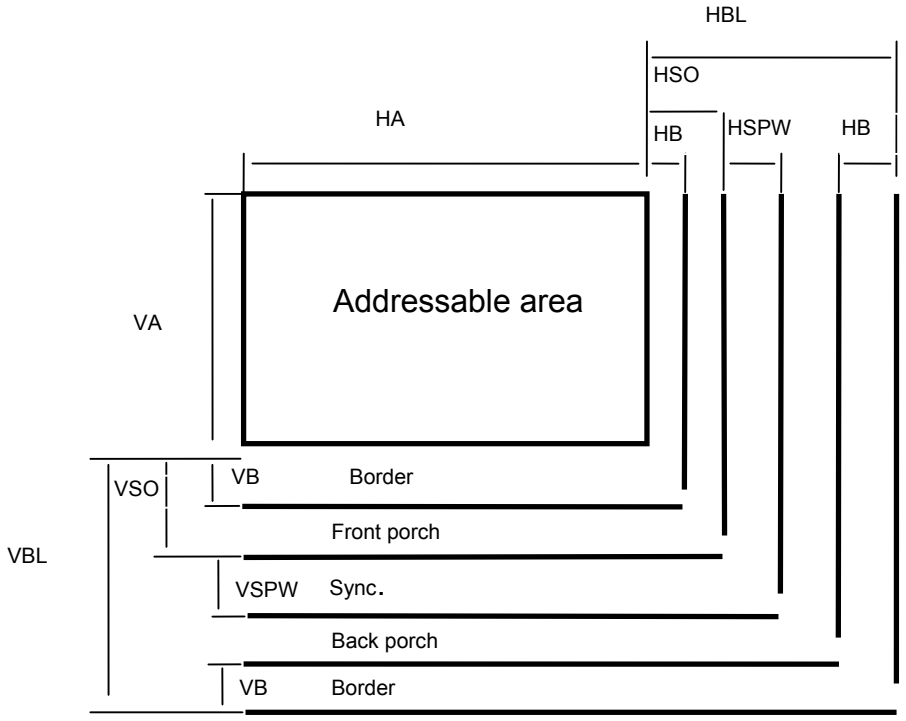
Address/Offset		Value (hex)	Value (binary)	Field Name and *Comments*
Byte # (decimal)	**Byte # (hex)**			
…	**…**	**…**		**…**
126	**7E**	00		**…**
127	**7F**	0A		Checksum: xxh ⇒ The 1-byte sum (modulo 256) of all 128 bytes in this VTB-EXT block is equal to zero.

©Copyright 1994 - 2003 Video Electronics Standards Association

4. APPENDIX B – Note Regarding Borders – (For Information Only)

This section is included to provide a frame of reference for the use of borders in detailed timings.

- Both the horizontal and vertical border sizes are for one side only. (i.e. the actual number of pixels or lines taken up by both borders is twice the listed value)
- Borders are assumed to be symmetric.
- Borders are not considered part of the active image time and do not affect the total line time, which should always be found by adding the active and blanking times for each axis.
- Borders may be part of the blanking time, but that portion that may be safely used to provide an illuminated solid-color border around the active image area.



VA	Vertical Active	HA	Horizontal Active
VBL	Vertical Blanking	HBL	Horizontal Blanking
VB	Vertical Border	HB	Horizontal Border
VSO	Vertical Sync. Offset	HSO	Horizontal Sync. Offset
VSPW	Vertical Sync. Pulse Width	HSPW	Horizontal Sync. Pulse Width

©Copyright 1994 - 2003 Video Electronics Standards Association

5. APPENDIX C – Data Formats – (For Information Only)

5.1 Video Timing Block Extension (VTB-EXT) High Level Layout

Refer to E-EDID Standard for the latest updates.

5.1.1 Mandatory elements

Block 0 (base 128 byte EDID table) is the only mandatory block.
This table shows the required use of E-EDID blocks.
All blocks are 128 bytes in length.
Each extension block is structured according to table 2-3 in section 2.1.3.
All extension blocks must be sequential, no holes allowed

Block #	Block Description
0	EDID 1.3 (or higher)
1	Extension if only 1 extension, otherwise EDID Block map (blocks 2-127)
2	Extension
3	Extension
4	Extension
:	
N	Extension
:	
128	EDID Block map for blocks 129 – 254 if more than 128 blocks used
129	Extension
:	
N =< 254	Extension

Table 5-1 – Extension Blocks – Mandatory Elements

Note: Block number 1 is used for Extension data if there is only one extension, otherwise block 1 is used as a block map.

©Copyright 1994 - 2003 Video Electronics Standards Association

5.1.2 EDID Block Map Extension

Byte #	Description	
0	Tag for Block Map	
1	Extension Tag for data in block 2 or block 129	Unused blocks are listed as Extension Tag = 0
2	Extension Tag for data in block 3 or block 130	
N	Extension Tag for data in block N+1 or block N+128	
126	Extension Tag for data in block 127 or block 254	
127	Check sum for this block map	

Table 5-2 – EDID Block Map Extension

Note: Block Tag is a byte that identifies the content of the Extension Block. A partial list of defined Tags is listed in Section 2.1.4.

5.1.3 General Extension Format

Byte #	Description	
0	Extension Tag	
1	Revision number for this tag	One byte binary number. Revisions are backward compatible.
2-126	Extension data	
127	Checksum for this Extension Block	

Table 5-3 – General Extension Format

©Copyright 1994 - 2003 Video Electronics Standards Association

6. APPENDIX D – Glossary

	Abbreviation	Meaning	Definition
1.	HA	Horizontal Active	The number of active pixels in a horizontal line that can be displayed in an image.
2.	HB	Horizontal Border	The number of in-active pixels in a horizontal line that occur during horizontal border time.
3.	HBL	Horizontal Blanking	The number of pixels in a horizontal line that occur during the horizontal blanking time.
4.	VA	Vertical Active	The number of active lines in a vertical field/frame that can be displayed in an image.
5.	VB	Vertical Border	The number of in-active lines in a vertical field/frame that occur during vertical border time.
6.	VBL	Vertical Blanking	The number of lines in a vertical field/frame that occur during the vertical blanking time.
7.	HSO	Horizontal Sync Offset	The number of pixels in a horizontal line that occur between the end of the horizontal active video and the beginning (leading edge) of the horizontal sync pulse. Also known as the horizontal front porch.
8.	HSPW	Horizontal Sync Pulse Width	The number of pixels in a horizontal line that occur between the beginning (leading edge) of the horizontal sync pulse and the ending (trailing edge) of the horizontal sync pulse.
9.	VSO	Vertical Sync Offset	The number of lines in a vertical field/frame that occur between the end of the vertical active video and the beginning (leading edge) of the vertical sync pulse. Also known as the vertical front porch.
10.	VSPW	Vertical Sync Pulse Width	The number of lines in a vertical field/frame that occur between the beginning (leading edge) of the vertical sync pulse and the ending (trailing edge) of the vertical sync pulse.
11.	HIS	Horizontal Image Size	The horizontal size (in millimeters) of the displayed image. Note: For projectors, the value of HIS is 0.0 mm.
12.	VIS	Vertical Image Size	The vertical size (in millimeters) of the displayed image. Note: For projectors, the value of VIS is 0.0 mm.

©Copyright 1994 - 2003 Video Electronics Standards Association

7. APPENDIX E - Answers To Commonly Asked Questions

Ref. #	Question	Answer
B-1	Why did VESA create the Video Timing Block Extension (VTB-EXT) Data Standard?	The base EDID definitions include four detailed timing blocks. During the past several years, industry requirements for these detailed timing blocks have limited their usefulness for additional video timings and monitor descriptors. EDID data structure (version 1, revision 3 or newer) definitions require the first detailed timing block to contain the preferred timing mode. Two of the detailed timing blocks must contain the monitor range limits and the monitor name. Some display manufacturers include a second video timing format or the monitor serial number in the fourth detailed timing block for asset management. Therefore, the base EDID table is full with little or no room for expansion. VESA created the VTB-EXT Data Standard to allow the industry to define additional video timings (up to six DTBs, 40 CVTs and/or 61 STs or a combination of DTBs, CVTs & STs) that are not available in the base EDID.
B-2	Can discrete monitor timings (DMT) be defined in the VTB-EXT block?	Yes, you can include DMTs in the VTB-EXT by defining standard timings. However, this is a duplication of video timing information (established timings & standard timings) that is already available in the base EDID. So doing this is not allowed. VTB-EXT should be used to define video timing formats that are not available in the VESA DMT Standard and are not defined in the base EDID table. The exception is the preferred timing mode (which can be a DMT) in the first detailed timing block of the base EDID table.

©Copyright 1994 - 2003 Video Electronics Standards Association