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VESA Display Device Data Block (DDDB) Standard

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Purpose

This proposal defines the Display Device Data Block (DDDB), for use in a CEA-861-compatible EDID extension, as originally proposed in the VESA TV Compatibility White Paper (Compatibility of PC and CE Displays, Aug.1, 2005).

Summary

VESA, working in cooperation with the Consumer Electronics Association (CEA), has proposed a convergence of the EDID extension definition used in both the PC and consumer electronics (TV) industries to describe monitor, TV, or 'multifunction' display products beyond the information provided by the base EDID file.

To achieve this, two new data blocks, compatible with the data block structure first defined by CEA-861-B, have been defined to replace the PC-only DI-EXT extension previously defined by VESA. This permits an extended EDID structure to be defined in a manner suitable for both industries, and containing information appropriate to monitor, television, and combined-use applications. Future use of the DI-EXT definition in PC displays is discouraged in favor of this compatible approach.

This standard defines a block which describes a number of additional characteristics of the display in question beyond that given in base EDID. The other new data block definition being established at this time is described in the VESA Display Transfer Characteristics Data Block (DTCDB) Standard.

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

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Revision History

September 25, 2006 – Initial Release of the Standard

1. Overview

This standard provides a definition for a fixed-length 32-byte data block, for use within an EDID extension as described by CEA standard entitled 'A DTV Profile for Uncompressed High Speed Digital Interfaces', also known as CEA-861. This definition is to be used as desired within such extensions as defined by CEA-861-C or later revisions.

This data block is intended to provide additional information regarding the display device's characteristics, beyond that which is provided by the base EDID definition established elsewhere by VESA (and which is also used under the CEA-861 standard). The information provided by this block most closely matches that provided in the earlier VESA Display Information Extension (DI-EXT) standard, but is defined here in a format compatible with the CEA-861 structure. (An additional data block definition, VESA DDDB, provides the enhanced response or "gamma curve" information that was also formerly provided by DI-EXT.) This permits the creation of EDID extensions that will meet the needs of both the consumer electronics/TV and personal computer industries, while remaining fully compatible with the CEA extension structure and readable by all host devices.

Note: Use of the earlier DI-EXT definition for new designs is not recommended, in favor of this CE/PC compatible system.

The specific information provided by this block includes a description of the video interface in use, its configuration and data rate limits; indications of support for content protection by the display; the horizontal and vertical dot or pixel pitch, and subpixel layout, configuration, and shape information for color displays; the default orientation of the display and its image scanning method; color and luminance encodings supported by this display, as well as the supported 'bit depth' for this data; over- and/or under-scan characteristics of the display; and other characteristics, features, and capabilities of the display not covered in the base EDID definition.

1.1 Display Device Data Block – Overall Description

The allocation of space within DDDB shall be as given in the table on the following page (table 1). Note that this block may, under the CEA-861 system, be located anywhere within the 128-byte extension which contains it; therefore, the addresses given in this table must be understood to be relative from the start of this particular block.

Only one Display Device Data Block may appear within the entire EDID structure (base EDID plus all extensions) provided by a given display; however, it is important to note that there is no requirement for this block to be provided by any display. Use of this data block may, however, be necessary to satisfy the requirements of other non-VESA standards or specifications.

1.2 Other Documents Referenced

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

Table 1-1: Reference Documents

Document	Version	Date
VESA White Paper – Compatibility of PC and CE Displays	NA	Aug. 1, 2005
VESA Display Information Extension (DI-EXT) Standard	Ver. 1	Aug. 21, 2001
VESA Enhanced Extended Display Identification Data (E-EDID) Standard	Rel. A, Rev. 1	Feb. 2000
VESA Enhanced Display Data Channel (E-DDC) Standard	Ver. 1.1	March 24, 2004
VESA Glossary of Terms		Latest version
VESA Monitor Control Command Set (MCCS) Standard	Ver. 2, Rev. 1	May 28, 2005
A DTV Profile for Uncompressed High Speed Digital Interfaces, CEA-861	C	August 2005

Table 1-2: Basic Display Device Data Block Structure

(Display Device Data Block - fixed 32-byte length. CEA block tag 7.2)

Rel. address (hex)	No. of bytes	Description
00	1	3 bit block tag (7h); 5 bits length (1Fh)
01	1	Child tag (02h) (identifies Display Device Data block)
02	1	4 bits Interface Type; 4 bits no. links/channels (if needed)
03	1	Interface Std. Version/release number (4 bits each)
04	1	Content protection support flags
05	2	Min/max clock frequency per link
07	4	Device native pixel format
0B	2	Aspect ratio & orientation
0D	1	Sub-pixel layout/configuration/shape
0E	2	Horizontal and vertical dot/pixel pitch
10	1	Misc. Display Capabilities
11	1	Audio
12	1	Audio delay
13	2	Frame rate/mode conversion
15	1	Color bit depth
16	8	Additional primary chromaticities
1E	1	Response time
1F	1	Overscan percentage

2. Detailed Specifications by Item

Note: All bits/bytes not explicitly defined in this section shall be considered as 'reserved' and should be set to zero in all implementations under this version of the standard.

2.1 Byte 00h – Data Block Tag and Block Length

This byte shall always contain the tag value 111 (decimal 7) in the first (upper) three bits, followed by five bits giving the length of the block as required by CEA-861C. As the length of the Display Device Data block is fixed at 32 bytes, the contents of this byte are fixed at FFh.

2.2 Byte 01h – Child Tag

This byte provides the child tag code, required for all tag 7 data blocks under CEA-861C. The child tag code which identifies this block is fixed as 02h.

2.3 Byte 02h – Interface Type/Number of Lanes or Channels

2.3.1 Interface Type

The first (upper) four bits of this byte shall contain a code, per the following table, which identifies the type of interface used by this display (as in use on the physical port from which the EDID structure containing this block was obtained). The number in parentheses is the permissible value for the number of lanes/channels for that interface, based on the current specification for the interface in question (see 2.3.2, below).

Table 2-1: Interface Type Codes

Code (hex)	Interface Type		Code (hex)	Interface Type
0	Analog (see exception in 2.3.2)		8	MDDI (1 or 2)
1	LVDS (generic) (any)		9	DisplayPort (1, 2, or 4)
2	RSDS (generic) (any)		A	IEEE-1394 (n/a – use 0 for number of lanes, see 2.3.2 below)
3	DVI-D (1 or 2)		B	M1, analog (n/a – use 0 for number of lanes, see 2.3.2 below)
4	DVI-I, analog section (n/a – use 0 for number of lanes, see 2.3.2 below)		C	M1, digital (1 or 2)
5	DVI-I, digital section (1 or 2)		D	Reserved
6	HDMI-A (1)		E	Reserved
7	HDMI-B (2)		F	Reserved

2.3.2 Number of Lanes/Channels

The lower four bits of this byte shall contain the number of lanes or channels provided by the interface identified in the Interface Type bits, with the definition of 'lanes' or 'channels' per the standard specification of that interface.

For example, a DVI interface may provide either one or two 'channels' as defined by the DVI specification, and therefore, the permissible values for this field in the case of a DVI interface is either '1' or '2' even though each 'channel' as defined by the DVI specification comprises three physical data pairs.

Note: The interface type field also permits definition of a generic TMDS interface, in which case the number of lanes or channels would be the actual number of physical data pairs used.

An exception to the above is made in the case of the Interface Type bits identifying an analog video interface (code 0h). In this case, the Number of Lanes bits are redefined to be a subtype code, which identifies the specific analog interface in use per the following table.

Table 2-2: Analog Interface Type Codes

Code (hex)	Interface Type		Code (hex)	Interface Type
0	15HD/VGA (VESA EDDC std. pinout – does not refer to the I2C protocol used in that standard)		8	Reserved
1	VESA NAVI-V (15HD)		9	Reserved
2	VESA NAVI-D		A	Reserved
3	Reserved		B	Reserved
4	Reserved		C	Reserved
5	Reserved		D	Reserved
6	Reserved		E	Reserved
7	Reserved		F	Reserved

2.4 Byte 03h – Interface Standard Version and Release Number

This byte shall contain the version (upper four bits) and release numbers (lower four bits) of the specification or standard document defining the interface associated with this EDID structure.

2.5 Byte 04h – Content Protection Support

This byte shall be used to define the available support for various content protection systems as may be supported on the interface associated with this EDID structure. As of this release, the following systems are recognized:

Table 2-3: Content Protection Codes

Code	Meaning		Code	Meaning
00h	No content protection supported		08h	Reserved
01h	HDCP		09h	Reserved
02h	DTCP		0Ah	Reserved
03h	DPCP (DisplayPort)		0Bh	Reserved
04h	Reserved		0Ch	Reserved
05h	Reserved		0Dh	Reserved
06h	Reserved		0Eh	Reserved
07h	Reserved		0F-FFh	Reserved

2.6 Bytes 05h, 06h – Minimum and Maximum Clock Frequency

These two bytes shall be used to define the maximum and minimum supported clock frequencies for the each link or channel of the interface defined by the contents of byte 02h of this block and presumed to be associated with this EDID data structure. The precise meaning of "clock frequency" here (i.e., whether this defines the pixel clock rate, the data rate on the physical interface, etc.) shall be assumed to be according to the definitions of the standard or specification controlling that interface type. The two bytes are allocated as shown in the following table.

Table 2-4: Max. and Min. Clock Frequency Bytes

Byte (offset)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	m5	m4	m3	m2	m1	m0	M9	M8
06h	M7	M6	M5	M4	M3	M2	M1	M0

Where m5:m0 represent a six-bit minimum clock frequency value, in MHz (range 0 – 63 MHz), and M9:M0 represent a ten-bit maximum clock frequency value, in MHz (range 0-1023 MHz). Note that it is not permissible for the maximum clock frequency value to be less than the minimum clock frequency value. Should both values be zero, the maximum and minimum clock frequency values shall be assumed to be the maximum and minimum as permitted under the appropriate interface specification or standard.

In the case of an analog interface, these values should be interpreted as the range of acceptable pixel rates.

In the case of a display interface which is elsewhere identified or specified as operating at a fixed frequency only, the minimum frequency value given in by 05h shall be ignored, and the maximum frequency information shall be assumed to be this fixed rate.

2.7 Bytes 07h through 0Ah – Device Native Pixel Format

These bytes describe the number of physical pixels in the horizontal and vertical directions, where those directions are defined relative to the local horizontal (i.e., floor, desktop, etc.) with the display in its normal or default orientation. (See Section 2.8 for the definition of bytes containing aspect ratio and orientation information.) If all bytes in this section are set to 00h, the display shall be assumed to be of a type which does not have a fixed pixel format (e.g., a typical CRT or vector-scan display).

Note: This information should NOT be used to infer the physical aspect ratio or size of the display, as there is no requirement that the physical pixels enumerated by these bytes are themselves of a 'square' (1:1) aspect ratio. If the display device is of a type in which the physical pixels are not arranged in an orthogonal/rectangular array (e.g., a 'delta-pixel' type), then these bytes shall contain the X and Y pixel counts of the "native" format of the display device, defined as the maximum number of image pixels which can be fully resolved (i.e., a 'checkerboard' pattern of this pixel count is resolvable by the device). Note that both the horizontal and vertical pixel counts are given as 16-bit values, to be interpreted as the pixel count on that axis, minus one; this provides a maximum permissible format of 65,535 x 65,535 pixels.

Table 2-5: Native Pixel Format Bytes

Byte (offset from start of block)	Description
07h	Horizontal pixel count, bits 0-7
08h	Horizontal pixel count, bits 8-15
09h	Vertical pixel count, bits 0-7
0Ah	Vertical pixel count, bits 8-15

2.8 Bytes 0Bh, 0Ch – Aspect Ratio & Orientation

These two bytes provide information on the physical aspect ratio (i.e., the ratio of the physical size of the long axis, relative to the shorter axis, of the image area of the display device) and default orientation of the display. Note that this is not necessarily the ratio of the physical or logical pixel count in these two axes, as given in the previous section, as the pixels may be 'non-square' (i.e., not of a 1:1 physical aspect ratio themselves).

The bytes are defined as shown in the following table.

Table 2-6: Aspect Ratio, Orientation, and Scan Direction Information

Byte (offset from start of block)	Description
0Bh	**Aspect ratio**; The aspect ratio is defined as the ratio of the physical dimensions of the image area of the display device, taken as long axis/short axis (and as such is a dimensionless quantity), expressed as a three-significant-figure value in the range of 1.00 to 3.55. The value stored here is given by: AR = (Long-axis image area size)/(Short-axis image area size) Stored value = (AR-1) * 100 For example, a display providing an image area of 160 mm x 90 mm (a 16:9, or 1.78:1, aspect ratio), would provide a value in this byte of 078 (decimal), or 4Eh. Note that this value is the same whether the "long side" of the image area is normally horizontal or normally vertical.
0Ch	**Default Orientation & Rotation Capability; Scan Direction** Note that all definitions in this section shall be with respect to the image area of the display, as seen by the user in the default or typical operating set-up and from the normal viewing position. **Bits 7,6 – Default Orientation** 00 – Landscape (long axis horizontal) 01 – Portrait (long axis vertical) 10 – Orientation not fixed (display may be rotated by the user; status information may need to be read "on the fly" to determine the current orientation.) 11 – Undefined. **Bits 5,4 – Rotation Capability** 00 – No rotation capability 01 – Display may be rotated 90 degrees clockwise from the default orientation described here. 10 – Display may be rotated 90 degrees counterclockwise from the default orientation described here. 11 – Display may be rotated 90 degrees in either direction from the default orientation described here. **Bits 3,2 – "Zero pixel" Location** The "zero pixel" is the screen location at which the scan begins for each new frame or field. This location is given as seen from the normal viewing position, with the display in its default orientation, per the following: 00 – Upper left corner 01 – Upper right corner 10 – Lower left corner 11 – Lower right corner Note that for a display which does not use a "raster scan" format, identifiable by the contents of Bits 1 and 0 (below), this information is irrelevant and the contents of these bits shall be ignored. **Bits 1,0 – Scan Direction** 00 – The scan direction for the display is not defined (e.g., a vector scan or other display type of indefinite scan direction & format). 01 – Fast (line) scan is along the long axis, slow (frame or field) scan is along the short axis. 10 – Fast (line) scan is along the short axis, slow (frame or field) scan is along the long axis. 11 – Undefined this code is reserved and not to be used at this time.

2.9 Byte 0Dh – Subpixel Information (Layout/Configuration)

Subpixel layout and configuration is identified by a code number as defined in the table below. This refers only to the subpixel physical layout and relative size of the features within each pixel; the actual physical size of the pixel is given in the next two bytes. A diagram in provided in Appendix A which shows typical examples, where appropriate, of the various defined layouts.

Wherever possible, it should be noted that this table is intended to be compatible with the code definitions used in the VESA Monitor Control Command Set (MCCS) Standard, Vers. 2, Rev. 1.

Table 2-7: Subpixel Layout Codes

Code	Meaning		Code	Meaning
00h	Subpixel layout is not defined.		08h	Mosaic (other)
01h	Red/Green/Blue vertical stripes (whether or not these stripes are continuous across the vertical dimension of the display screen).		09h	Quad subpixels; a 2 x 2 subpixel structure including one each of red, green, blue, and one additional color, including white, in any order[1].
02h	Red/Green/Blue horizontal stripes (whether or not these stripes are continuous across the horizontal dimension of the display screen).		0Ah	Five subpixels, including RGB subpixels aligned as in the case of 01h, with two additional subpixels located above or below this group[1].
03h	Vertical stripes (as in 01h), with the primary ordering given by the order of the chromaticity information in the base EDID.		0Bh	Six subpixels; as in case of 0Ah, but with three additional colors in addition to the base set[1].
04h	Horizontal stripes (as in 02h), with the primary ordering given by the order of the chromaticity information in the base EDID.		0Ch	Clairvoyante, Inc. PenTile Matrix™ layout[2] (see drawing in Appendix A).
05h	Quad subpixels; a 2 x 2 structure with a red subpixel at top left, a blue subpixel at bottom right, and the remaining two subpixels green.		0Dh	Reserved for future use.
06h	As in 05h, but with red at bottom left and blue at top right.		0Eh	Reserved for future use.
07h	Delta (triad) RGB subpixels.		0F-FFh	Reserved for future use.

Note 1: In the case of layouts providing more than three subpixels, the color coordinates of the additional subpixels shall be described as specified in section 2.16.

2.10 Bytes 0Eh, 0Fh – Horizontal and Vertical Dot/Pixel Pitch

As used in this standard, ‘dot pitch’ or ‘pixel pitch’ shall be understood to mean the distance from the geometric center of any given dot or pixel on the physical display screen, to the geometric center of the nearest adjacent dot or pixel, along the specified axis (horizontal or vertical). In the case of either of these values being zero, it shall be assumed that there are no discrete dot or pixel structures in the display screen along that axis (e.g., in the case of an aperture-grille CRT in which the grille apertures are aligned with the vertical axis of the tube, the vertical pitch is zero).

If both pitch values are given as zero, it shall be assumed that the display device in question does not have a discrete pixel structure (e.g., a monochrome CRT) or is a projection display (which has no fixed pixel pitch in the displayed image). In the case of a display which does not have a fixed orientation (e.g., a ‘pivotable’ display which may be used as either a landscape- or portrait-format device), the meaning of "horizontal" and "vertical" shall be as these apply in the default orientation of the product, as identifiable elsewhere in the EDID data structure.

In the case of a display with a variable dot or pixel pitch, the average value shall be given here.

Table 2-8: Horizontal and Vertical Dot/Pixel Pitch Bytes

Byte (offset)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Horiz. pitch, in increments of 0.01 mm (range 0.00 to 2.55 mm)							
0Fh	Vertical pitch, in increments of 0.01 mm (range 0.00 to 2.55 mm)							

It is important to note that stating the horizontal and vertical dot or pixel pitches in this manner should not be interpreted as implying that the display screen comprises a rectilinear array of pixels; the configuration and shape of the pixel and subpixel structures are given elsewhere in this data block.

2.11 Byte 10h – Miscellaneous Display Capabilities

This byte provides flags indicating support for various display capabilities, as defined in the following table.

Table 2-9: Miscellaneous Display Capabilities Flags

Byte (offset)	Bit no.	Definition
10h	7, 6	*Dithering*: These two bits describe the type of "dithering" (temporal and/or spatial modulation of luminance levels) to achieve increased dynamic range, if any, used by the display device, per the following: 00 – No dithering used. 01 – Spatial dithering only. 10 – Temporal dithering only. 11 – A combination of spatial and temporal dithering is used.
	5	*Direct-drive:* If set ('1'), this bit indicates that the display device associated with this EDID structure is of the 'direct-drive' type, meaning that the external interface feeds the display device (e.g., LCD panel) directly, and that there is no scaling, de-interlacing, frame-rate conversion, etc., between this interface and the panel or other display device.
	4	*Overdrive not recommended*: If set, the video source shall not by default apply "overdrive" in creating the video signal to be provided to the display in question. (E.g., this permits a display which already incorporates "overdrive" in the panel or controller to prevent the video source from duplicating this, which might result in visible artifacts.)
	3	*Deinterlacing*: If set ('1'), the display has the capability to deinterlace any interlaced video input and display it in a progressive-scan format. If cleared ('0'), then the display does not have this capability.
	2	Reserved at 0
	1	Reserved at 0
	0	Reserved at 0

2.12 Byte 11h – Audio

This byte provides flags which indicate the presence of support for various audio features or functionality in the display device associated with this EDID structure.

Table 2-10: Audio Flags

Byte (offset)	Bit no.	Definition
11h	7	*Audio support on video interface*: If set ('1'), audio is supported on the video interface associated with this EDID structure (if permitted under the interface standard in question).
	6	*Separate audio inputs provided*: If set ('1'), audio inputs are provided separately from the video interface associated with this EDID structure. (Note that it is permissible for both bits 7 and 6 to be set to '1.')
	5	*Audio input override*: If set ('1'), then audio information received via the video interface associated with this EDID structure will automatically override any other audio input channels provided and will be routed to the appropriate audio output devices or connectors.
	4 - 0	Reserved at 0

2.13 Byte 12h – Audio Delay

This byte indicates the relative delay of audio through the display device (if audio support is provided) vs. the display of video information.

The delay value given here is the absolute offset between the audio and video signals, assuming that these are perfectly in sync as delivered to the display's inputs, per the requirements of the audio/video interface(s) in question (whether the audio and video are carried on separate physical interfaces or combined in any manner on to a single physical connection). In this case, the delay value is given in milliseconds (range 0-254 ms), with a resolution of 2 ms.

The value given is the inherent difference in latency between the display's video and audio signal paths, *without* any delay compensation within the display (if available) enabled (unless such compensation is always active, and is not subject to enabling/disabling or other control by the user or video source device).

Table 2-11: Audio Delay

Byte (offset)	Bit no.	Definition
12h	7	*'Sign' bit*: If set ('1'), this bit indicates a 'positive' delay; i.e., the audio material is presented later than the video. If cleared ('0'), this indicates a 'negative' delay; i.e., the audio material is presented earlier than the video.
	6-0	Audio delay divided by 2. A value of 0 shall indicate that the video source should not attempt to provide any compensation for the display's audio delay. If the delay is greater than 254 milliseconds, the value shall still be stored as 127.

Note: This effectively uses 'sign-magnitude' notation to provide the delay; this form of notation has the peculiarity of having two ways to represent a zero value, in this case '00h' and '80h'.

For this specification, the '00h' representation is special-cased and shall be interpreted as 'no delay information provided'. Should a display device need to actually indicate zero delay between audio and video, this byte should contain '80h'.

2.14 Bytes 13h, 14h – Frame Rate/Mode Conversion

These bytes are used to indicate support for the conversion of incoming video information from its current frame rate to the frame rate at which the display panel or other device is actually operated, should these be different. The second of these (byte 14h) gives the native or nominal frame rate at which the display device actually operates, if this is fixed.

Table 2-12: Frame Rate/Mode Conversion

Byte (offset from start of block)	Description
13h	**Note:** If NONE of the bits in this byte are set to '1' (i.e., the contents of this byte are 00h), then no support for frame rate conversion or operation at non-native rate is provided by the display device; the device must be operated at the native rate specified below and/or in the Preferred Timing information to ensure a usable image. **Bits 7-6** 00 – No dedicated rate conversion hardware is provided; the display device, however, will operate 'natively' over the range given in these bytes. 01 – The display provides a single frame buffer or utilizes some other technique such that the input frame rate and the frame rate of the display device are not required to be the same, but tearing or other artifacts may be visible if the input and display frame rates are not matched. 10 – The display provides double-buffering or some other method such that input frames may be dropped or duplicated in order to affect the conversion between input and display device rates. 11- The display provides frame-rate conversion involving interframe interpolation or some other technique more advanced than simple duplication or dropping of entire input frames.

	Bits 5-0 – *Device Frame Rate Range:* In the case of a display in which the actual display device is not operated at a rigidly fixed rate, but rather has a permissible range of "native" operation, these bits are used (along with the nominal value given in the following byte) to indicate that range. The value given here is the maximum excursion permissible, assuming a range centered on the nominal rate given below (i.e., the device is capable at operating over a range given by *Device Nominal Rate* ± *Device Frame Rate Range).* The maximum value possible in six bits is 63. Therefore the maximum range possible is ± 63 FPS about the nominal value. (See note)
14h	*Device Native or Nominal Rate:* The value of this byte (range 0 to 255) gives the frame rate (in frames/sec) at which the display device (panel, etc.) itself operates, or, if bits 5-0 in the preceding byte contain a value other than 0, the center of the range of frame rate range as described above. (See note)

Note: In the case of a display device which normally operates in an interlaced mode, or other mode such that the entire frame is not updated in a single pass, the value of bits 5-0 of byte 13h and the value of byte 14h shall be interpreted in fields/second.

2.15 Byte 15h – Color Bit Depth

This byte is used to indicate the color 'bit depth' (i.e., effective dynamic range) provided for each color. It is assumed that the bit depth of all primaries (typically at least red, green, and blue) are the same. Two separate values are provided here; bits 7-4 give the bit depth, minus 1 (i.e., range 1-16) per primary which is supported on the display interface associated with this EDID structure. Bits 3-0 give the bit depth, minus 1 (again, range 1-16) per primary which is provided per frame (i.e., without the effects of frame-to-frame modulation or "temporal dithering" considered) at the display device (e.g., LCD panel or similar).

Table 2-13: Color Bit Depth

Byte (offset)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15h	Color Bit Depth – Interface				Color Bit Depth – Display Device			

2.16 Byte 16h through 1Dh – Additional Primary Chromaticities

These eight bytes provide a means for specifying the color coordinates of up to three additional 'primary' colors, over and above the base set as defined in bytes 19h through 20h of the base EDID structure (as currently specified E-EDID Release A, Rev. 1).

The same format as is used in the base EDID colorimetry bytes is followed here, with the exception that there is no "white point" information given.

Note: All information given is in terms of the 1931 CIE *xy* color space coordinates; ten bits of accuracy is provided for both coordinates in all colors given. If a given primary is not provided by the display in question (i.e., a display with four or five primaries, total, of the possible six), the bits corresponding to the coordinates for the unused primary or primaries shall be set to zero. Bits 1 and 0 of Byte 18h shall also be used to indicate the number of additional primaries provided by the display.

Also note that the ordering of the chromaticity information given here is also used to identify the color of subpixels in some cases of the Subpixel Information code given in byte 0Dh, as described in section 2.9.

For further information, please see that section and the subpixel layout diagrams given in Appendix A of this specification.

Table 2-14: Additional Primary Chromaticities

Byte (offset from start of block)	Description (Note: '4x1' indicates bit 1 of the *x* coordinate of Primary 4, etc.)			
	Bits 7, 6	**Bit 5, 4**	**Bits 3, 2**	**Bits 1, 0**
16h	4x1, 4x0	4y1, 4y0	5x1, 5x0	5y1, 5y0
17h	6x1, 6x0	6y1, 6y0	(reserved at 0)	Number of add'l primaries
18h	Primary 4, *x* coordinate, bits 9-2			
19h	Primary 4, *y* coordinate, bits 9-2			
1Ah	Primary 5, *x* coordinate, bits 9-2			
1Bh	Primary 5, *y* coordinate, bits 9-2			
1Ch	Primary 6, *x* coordinate, bits 9-2			
1Dh	Primary 6, *y* coordinate, bits 9-2			

Note: The base set (typically red, green, and blue, in that order) are considered to be primaries 1-3 in this numbering, and their color coordinates are, as mentioned above, already provided in the base EDID.

Primaries 4 through 6, described here, may be of any color (including white), and there is currently no standard ordering for these. This numbering system is also used to identify the colors of corresponding physical subpixels in some subpixel layouts as defined in section 2.9 (byte 0Dh).

2.17 Byte 1Eh – Response Time

This byte is used to indicate the response time of the display device associated with this EDID structure, as follows. The value stored should be the worst-case response time associated with this display device.

Table 2-15: Response Time Information

Byte (offset)	Bit no.	Definition
1Eh	7	If this bit is cleared ('0'), then the value given here is for a 'black to white' (lower gray value to higher) transition; if set ('1'), the value is for a 'white to black' (higher to lower) transition.
	6-0	Response time value (ms). If the response time is any value less than 1 ms, a value of "0" shall be stored here. Similarly, if the response time is any value greater than 126 ms, a value of "127" shall be stored here.

2.18 Byte 1Fh – Overscan Information

This byte shall be used to provide information relating to the usage of the visible physical screen area vs. the active area of the image. If, in the default mode of operation of the display device, the active image extends beyond the limits of the visible physical screen of the display device, an 'overscan' condition exists. This byte is used to describe the extent of that overscan, i.e., the amount of active image "lost" to the viewer by virtue of being outside the visible screen area.

The contents of this byte shall be interpreted as shown in the table below.

Table 2-16: Overscan Information

Byte (offset)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Fh	Horizontal %				Vertical %			

Bits 7-4 – Four bits indicating the percentage of overscan in the horizontal direction (where 'horizontal' is assumed to be as in the default orientation of the display device, and therefore in the same direction as 'horizontal' image or screen size information given elsewhere in the EDID structure).

This value is to be the percentage of the active image which is located outside the visible screen on either side of the display (i.e., if a total of 10% of the image, horizontally, extends beyond the visible screen area, then assuming a properly-centered image would mean a 5% overscan on either side), rounded to the nearest integer percentage value, i.e., the range of this four-bit value is 0 to 15%.

Should a value of "0%" be given here, it shall be assumed that the entire active image is visible; however, this does not necessarily mean that the image exactly fills the visible screen area (i.e., an 'underscan' condition may exist in which the active image is smaller than the visible screen area; this is not specifically indicated here).

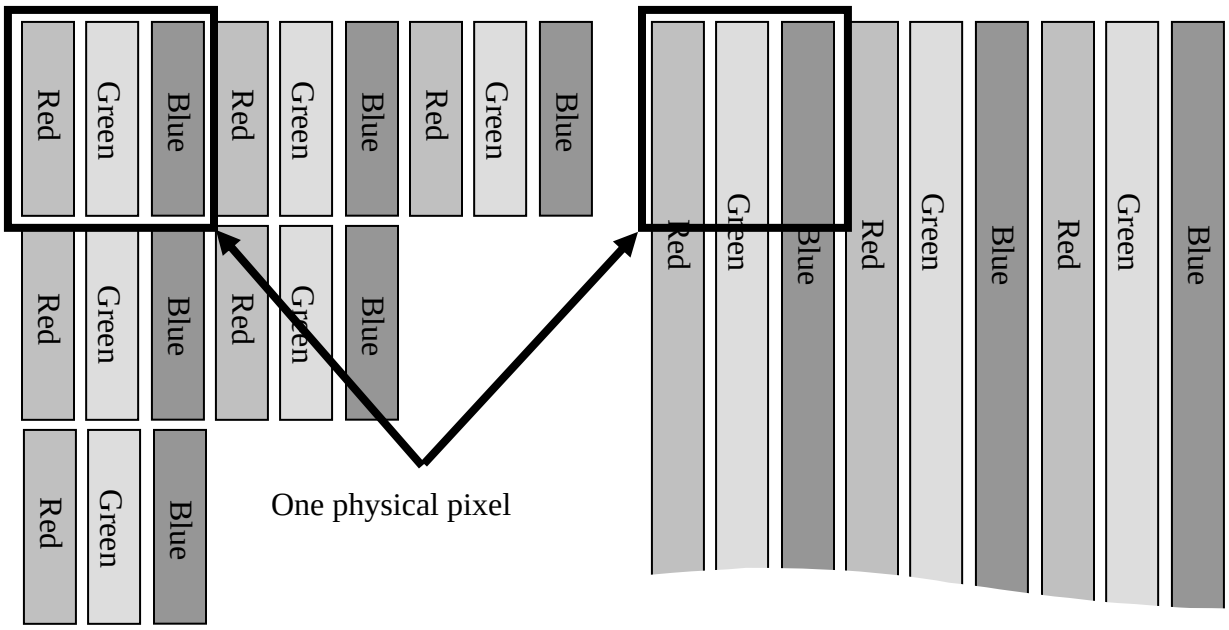
Bits 3-0 – As above, but in this case the vertical overscan percentage (where 'vertical' is again assumed to be as in the default orientation of the display device, and therefore in the same direction as 'vertical' image or screen size information given elsewhere in the EDID structure).

Appendix A – Subpixel Layout Examples

The VESA Display Device Data Block provides a means for conveying the subpixel layout (i.e., the arrangement of individual color areas within a physical pixel) of the display device in question, as defined in section 2.16.

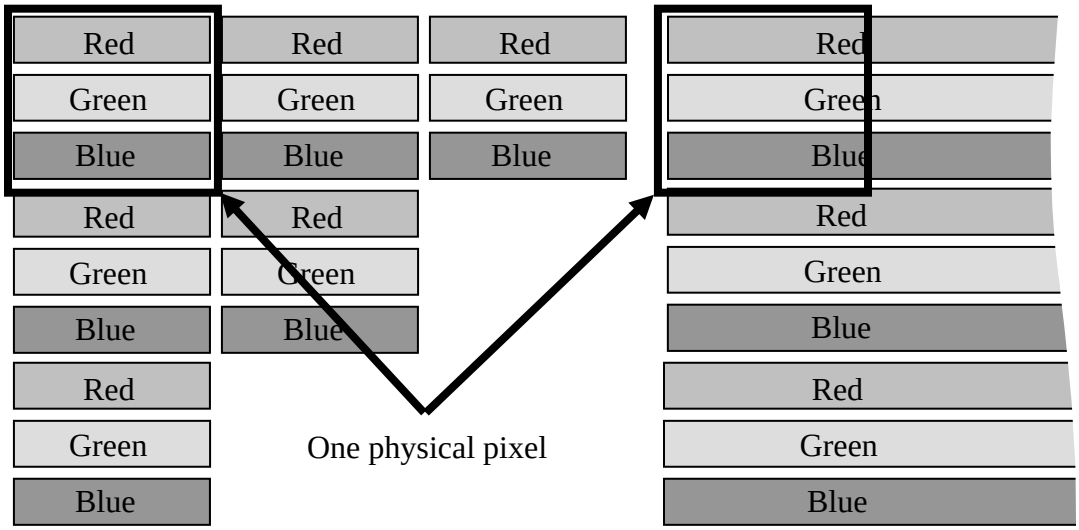
This appendix provides pictorial examples of the layouts assigned a subpixel layout code in that section. If there is any conflict between the information provided here and the contents of section 2.16, that section shall take precedence.

Code 01h – RGB Vertical Stripes



Code 01h applies to either individual pixels (left) or continuous vertical stripes (right).

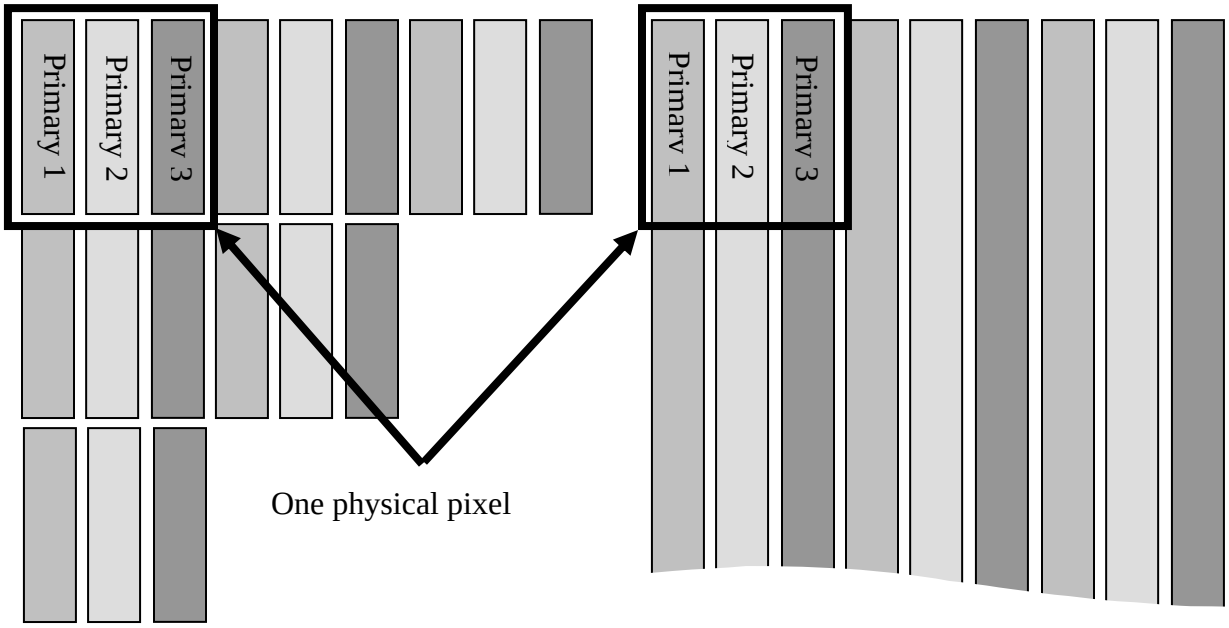
Code 02h – RGB Horizontal Stripes



Code 02h applies to either individual pixels (left) or continuous horizontal stripes (right).

Codes 03h, 04h – Vertical/Horizontal Stripes with Non-standard Primary Ordering

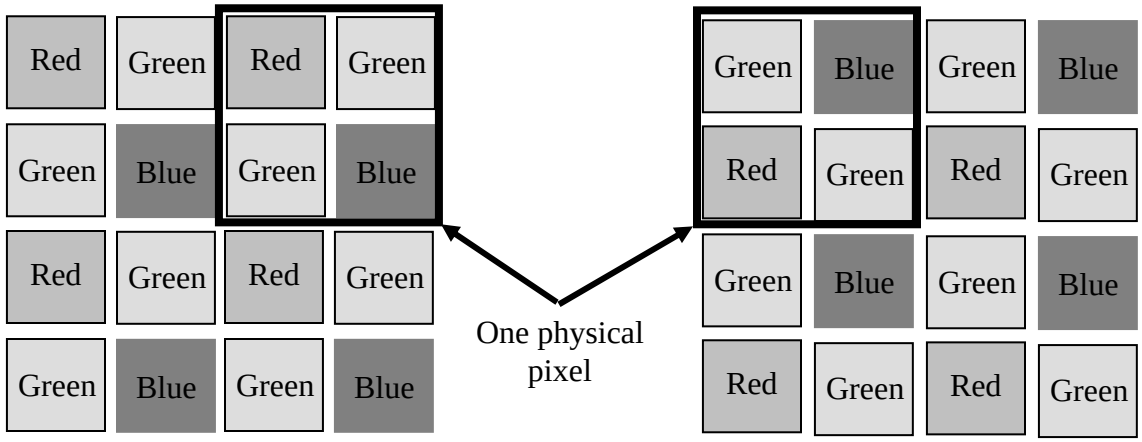
These codes refer to pixel layouts which are physically identical to those described as (01h) and (02h), above, with the exception that the ordering of the primaries are not as shown above. Instead, the ordering will be as determined by the order of chromaticities provided in the base EDID, as shown below:



Primary assignments for code 03h. Code 04h is the same but for horizontally-oriented primary "stripes," with the assignments of primaries in the same manner – the primary listed first in the base EDID ("Primary 1") in the areas originally defined as "Red," "Primary 2" in the areas originally defined as "Green," and "Primary 3" in the areas originally assigned to "Blue."

Codes 05h, 06h – Quad Subpixels

These codes refer to pixel layouts which use a 2 x 2 square array of subpixels; they differ in the relative location of the primaries, as shown below.

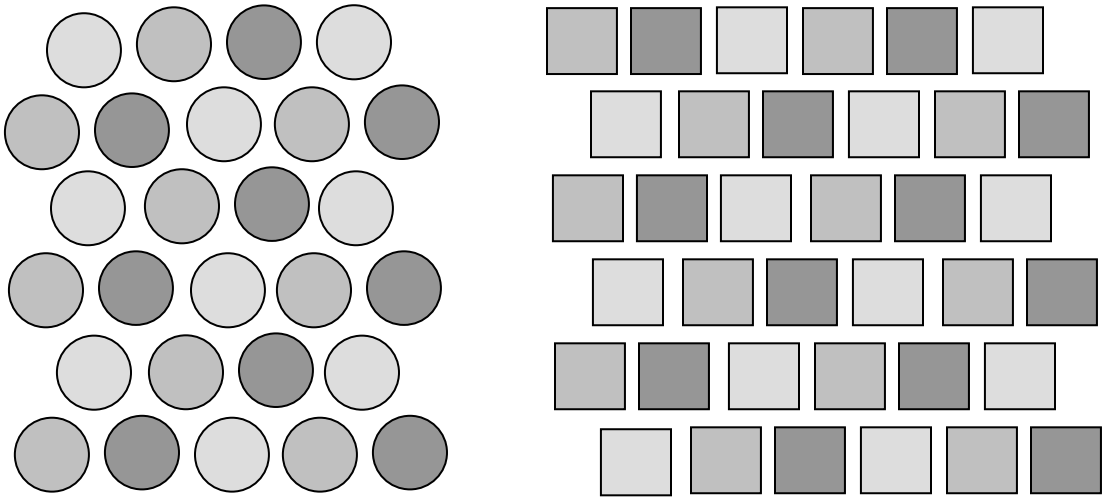


Layout Code 05h

Layout Code 06h

Code 07h – Delta Subpixels

This code refers to layouts involving tri-color (RGB) subpixels, either round or square, arranged in a "delta" pattern as shown below.

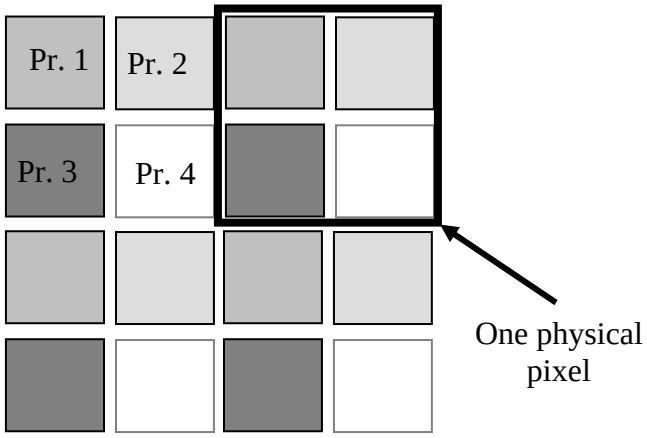


Code 08h – Mosaic (other)

This code is used to identify other subpixel layouts which do not conform to any of the standard descriptions given here.

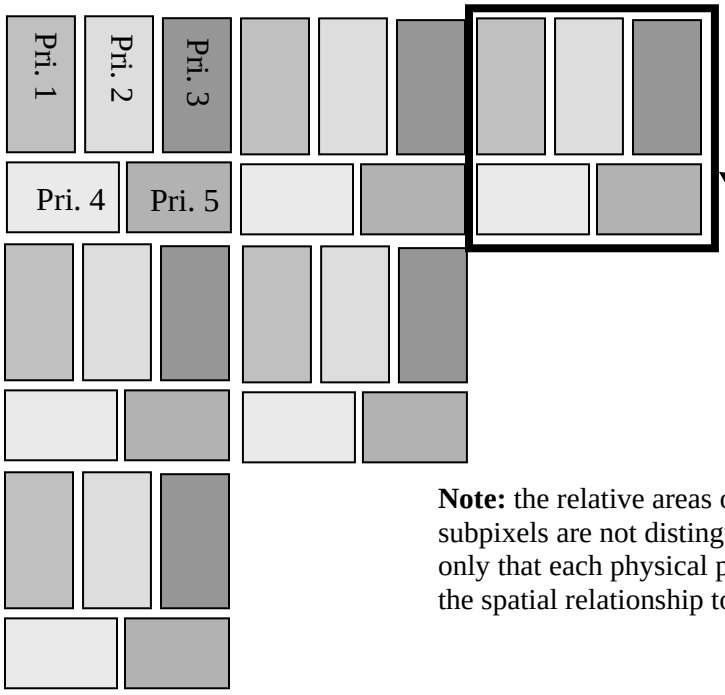
Code 09h – Quad Subpixels, RGBW or RGBx

This code describes a 2 x 2 subpixel structure including one each of the typical R, G, and B primaries, in the order given by the order of chromaticities (1, 2, 3) as given in the base EDID, plus one additional color (which may be of any other color, including white, with the chromaticity given in the "Additional Primary Chromaticities" section of this block, as "Primary 4").



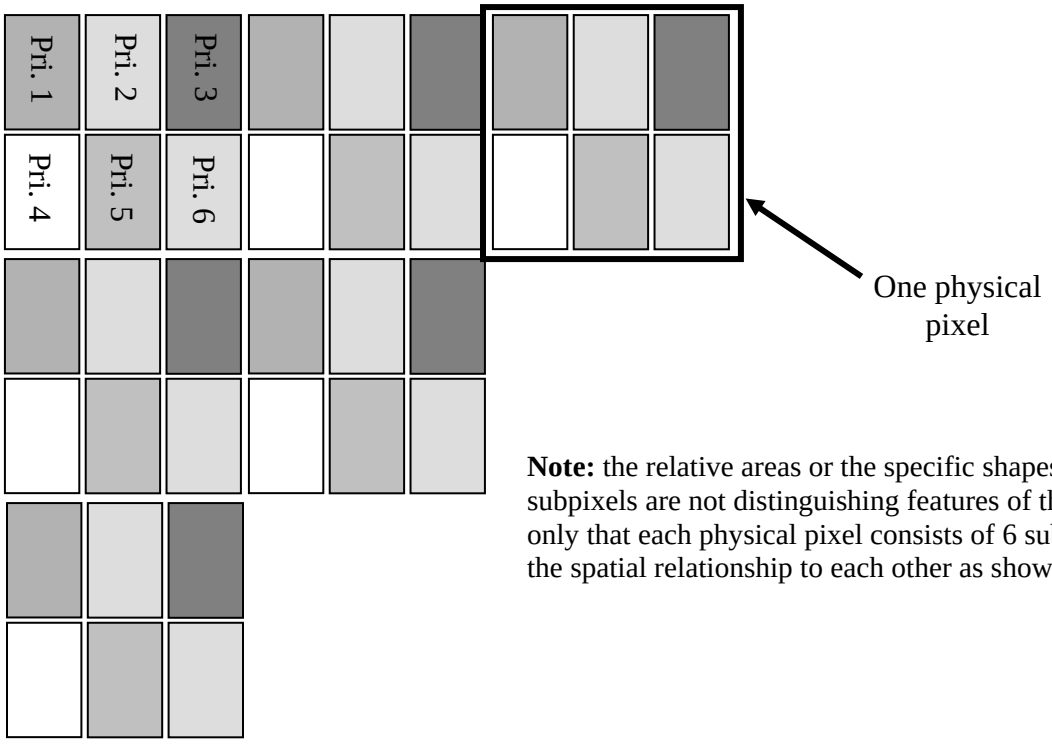
Code 09h – Quad Subpixels

Code 0Ah – Five Subpixels, 3 + 2 Layout



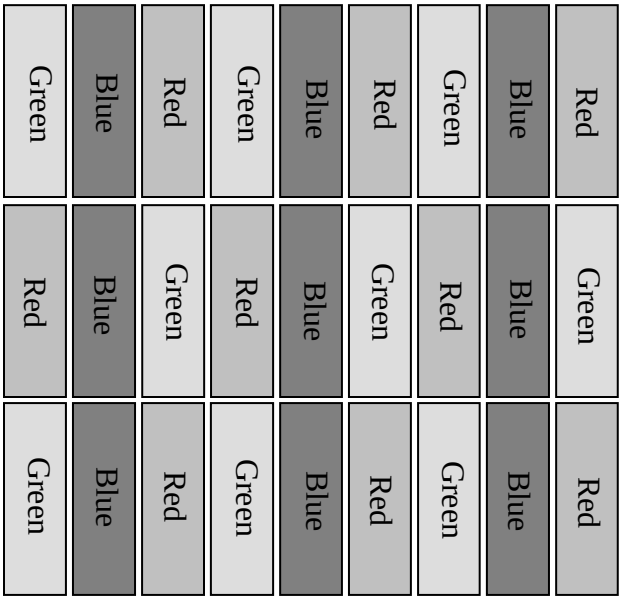
Note: the relative areas or the specific shapes of the subpixels are not distinguishing features of this layout, only that each physical pixel consists of 5 subpixels in the spatial relationship to each other as shown here.

Code 0Bh – Six Subpixels



Note: the relative areas or the specific shapes of the subpixels are not distinguishing features of this layout, only that each physical pixel consists of 6 subpixels in the spatial relationship to each other as shown here.

Code 0Ch – Clairvoyante, Inc., "PenTile Matrix"™



Note: In the Clairvoyante system, there is no *fixed* assignment of a given set of subpixels to form a unique physical pixel; subpixels are used to create complete "physical" pixels in various combinations, under the control of the drive electronics.

Appendix B – Sample Display Device Data Block

The following provides an example of a typical Display Device Data Block. This example is not intended to represent any particular actual product.

Address (offset within block)	Value	Description
00h	FFh	Upper three bits: tag code (111); lower five bits: length (11111)
01h	02h	Child tag code (fixed by data block definition)
02h	92h	Interface type and numbers of lanes; this device identifies itself as using the DisplayPort interface (upper four bits, code 9h) and supporting 2 data lanes (lower four bits).
03h	11h	This data block complies with Version 1, Release 1 of the Display Device Data Block specification.
04h	03h	Device supports DPCP content protection.
05h	00h	Minimum and maximum interface clock frequency information. Since this device has identified itself as using the DisplayPort interface, the zero values for both minimum and maximum indicate that the clock rate limits are per that specification, and not given explicitly here.
06h	00h	
07h	00h	Horizontal pixel count, device native format. Byte 07h gives the lower eight bits of this value, while byte 08h gives the upper eight bits. The horizontal pixel count is therefore 0A00h, or 2560 pixels.
08h	0Ah	
09h	40h	Vertical pixel count, device native format. Byte 09h gives the lower eight bits of this value, while byte 0Ah gives the upper eight bits. The vertical pixel count is therefore 0640h, or 1600 pixels.
0Ah	06h	
0Bh	3Ch	Aspect ratio. This is a 2560 x 1600 display providing physically "square" pixels, and so it has an aspect ratio of 16:10, or 1.6:1. This is encoded in this byte as the decimal value 60 [(1.60 -1) * 100], or 3Ch
0Ch	11h	Orientation and scan direction. The contents of this byte are read as four two-bit pairs; starting from the MSBs (bits 7 and 6) to the LSBs (1 and 0), these are: 00 – the default orientation of the device is landscape (long axis horiz.) 01 – the device may be rotated 90 degrees clockwise from the default 00 – the 'zero pixel' is in the upper left corner when in the default orientation. 01 – The fast (line) scan is along the long axis of the device, while the slow (frame or field) scan is along the short axis. (I.e., along with the previous two bits, this indicates that the device operates in the conventional manner, with the faster scan axis being horizontal and scanned left-to-right, while the slower scan axis is the vertical, and is scanned top-to-bottom.
0Dh	0Ah	Sub-pixel layout and configuration. The value of 0Ah indicates that this display provides five sub-pixels per pixel (see Appendix A for examples of the pixel configurations). The chromaticities of the first three sub-pixels (as identified in Appendix A) are given as the primary colors contained in the base EDID; the chromaticities of the remaining two sub-pixels will be given in bytes 16h plus

		18h through 1Bh in this data block.
0Eh	18h	Horizontal pixel pitch. This display has a horizontal pixel pitch of 0.24 mm, so the value stored here is decimal 24, or 18h.
0Fh	18h	Vertical pixel pitch. This display has a vertical pixel pitch of 0.24 mm, so the value stored here is decimal 24, or 18h.
10h	D0h	Miscellaneous display capabilities. In binary, the contents of this byte are 11010000, which is interpreted per Sect.
11h	80h	Audio flags. Bit 7 is set, indicating that audio is supported on the video interface (in this case, DisplayPort); bits 6 and 5 are cleared, indicating that there are no separate audio inputs provided (bit 6) and that there is no automatic override of separate audio inputs (bit 5). Bits 4-0 are reserved at 0 as of this version of the data block specification.
12h	13h	Audio delay. Bit 7 is set, indicating that this is a "positive" delay (i.e., the audio material will be presented later than the video, if no compensation is performed); bits 6-0 give the magnitude of this delay, in this case 6 ms (the stored value is the actual delay divided by 2).
13h	8Fh	Frame rate/mode conversion information & frame rate range. The upper two bits in this byte are 10, indicating that the display device provides a double-buffered frame rate conversion mechanism. The lower six bits are 001111 (0Fh), indicating that the frame rate range is ±15 Hz from the nominal rate given in byte 14h, below.
14h	3Ch	Device nominal native frame rate; 3Ch = 60 decimal, or 60 Hz.
15h	88h	Color bit depth. The upper four bits give the depth, in bits/color, supported on the device's video interface, while the lower four give the same information for the display device (transducer) itself. In this case, both the interface and the transducer are operating at an effective dynamic range of 8 bits/color.
16h	41h	Lower bits of chromaticity data for Primaries 4 and 5 (see full explanation below, for bytes 18h through 1Dh).
17h	02h	Chromaticity coordinates (lower bits) of Primary 6, plus two bits reserved at zero, plus the number of additional primaries given in the bottom two bits of the byte; as this is a five-subpixel device, this section of the block contains two "additional" primaries (over the standard three listed in the base EDID data), and therefore this byte contains 02h (no data for Primary 6, plus the number of additional primaries (2)).
18h	35h	Chromaticity coordinates (upper 8 bits) of the additional primaries. This device provides two additional primaries (in additional to the three defined in the base EDID data: a cyan primary at CIE *xy* coordinates of (0.1457, 0.2893), and yellow at (0.4931,0.4662). As in the base EDID definition, all values are stored to ten-bit accuracy, as binary fractions. For these colors, then, the values to be stored are: Cyan: (.0010010101, .0100101000) Yellow: (.0111111000, .0111011101) These are stored with the upper eight bits of the cyan (primary 4) *x* value in byte 18h, the upper eight bits of the cyan *y* value in 19h, and the upper eight bits of the yellow (primary 5) *x* and *y* in bytes 1Ah and 1Bh, respectively. The lower two bits of all of these values are stored in byte 16h, per the assignment in section
19h	4Ah	
1Ah	7Eh	
1Bh	77h	

1Ch	00h	2.16. As there is no sixth primary, bytes 1Ch and 1Dh contain no information and are set to 0.
1Dh	00h	
1Eh	1Ch	Response time. The response time given here is for a white-to-black transition, and has a value of 12 ms.
1Fh	57h	Overscan: 5% horizontal, 7% vertical